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EE 252 Electronics 2 Fall, 2017

Text: Donald A. Neamen, *Microelectronics Circuit Analysis and Design,* McGraw Hill, 4th ed.
Suggested: Tront, *PSpice for Basic Microelectronics*, McGraw Hill (with CD)
Cadence ORCAD/PSpice circuit simulation software (available in SLC216, SLC224, …)
Engineering Laboratory Reports Manual (provided)
Scheduled class times: MWF 11:00-11:50 SLC222; Lab: W1:00-3:50 or M12:00 – 2:50 SLC224
Instructor: John B. Gilmer Jr. Office hours: TBD Office: SLC220 Phone: x4885
Prerequisites: EE251 Electronics 1, EE283 Measurement Lab, MTH112 Calculus 2, PHY202.

Bulletin Description:

EE-252. Electronics II

Credits: 4

Multi-transistor amplifiers, operational amplifiers. Frequency response and the design of filters and amplifiers to meet frequency specifications. Feedback in amplifier design and oscillators. Three one-hour lectures and one three-hour lab per week.

Pre-Requisites EE-251, EE-283, MTH-112, and PHY-202.

"Outcomes" sought:

1. Students will be able to analyze and design CMOS and BJT circuits, and model them with simulation.
2. Students will be able to describe the operation of, analyze, and design different types of amplifiers.
3. Students will be able to analyze and design filter circuits, and simulate them.
4. Students will be able to analyze and design [operational] amplifier circuits and simulate them.
5. Students will be able to describe the trade-off between gain and bandwidth in negative feedback amplifiers along with the effect on input and output impedance.
6. Students will be able to analyze feedback loops for stability.

Background:

As a continuation from Electronics 1, this course will continue to focus on electronic devices and their use in circuits to accomplish fundamental functions such as amplification and filtering. However, we will be moving toward a greater concern for the way various functions fit together to form an overall system, and assessment of overall performance, especially in the frequency domain.

In this course, the emphasis is on analog electronics. We will focus particularly on different approaches to what is perhaps the most basic electronic function, the amplification of signals, often with tailored frequency responses to filter out undesired frequencies. Even in an age where digital electronics are becoming more important, analog electronics are still needed to amplify signals to a level where they can be converted into digital form. At higher frequencies, and in lower cost applications, there is no alternative to an analog approach. When a signal needs to be amplified to power levels beyond that of digital microelectronics, such as to drive a speaker or antenna, analog electronics is usually used. Many of the functions digital circuits seek to accomplish emulate analog functions, a further reason to study analog circuits. Finally, at high speeds, understanding digital electronics requires analog concepts and techniques.

My own interest in electronics began when I was in 4th grade. My aunt gave my mother a paperback book on how to fix your own TV set. Ours had good sound, but the picture was broken up into a hash of diagonal lines. The book explained how a television set worked, and how you could diagnose the problem and fix it by replacing a vacuum tube, the failed electronic component. I recall as early as 6 years old or so wondering how those pictures could get inside

the TV set and be presented on the front, but none of my imagined contrivances for moving pictures around could explain it. Here, suddenly, was the answer! I now understood, at least in a general sense, how the TV worked. It was exciting, and sparked an interest in electronics, and how such things work, that has carried me to this day. In this course, I hope to give you the opportunity to understand and appreciate such things.

The fundamentals of analog television changed very little since that year around 1959 when I first learned how it worked. The signals remained much the same, and the receivers worked the same way, though with solid state rather than vacuum tube electronics. (Be thankful for transistors! When I was young, I routinely worked with circuits that operated at about 250 Volts or more!) But Television has now finally changed fundamentally, with high definition and digital television replacing the old format, and cathode ray tubes nearly all gone. Yet, many of the basic elements are still needed. A superheterodyne receiver still performs the task of amplifying the weak signal from the antenna, and shifting it down into a frequency range that digital electronics can handle, and selecting the narrow band of frequencies associated with a single station. Power switching circuits still supply needed voltages. Power amplifiers to drive the display and speakers are still needed. The world still needs analog electronics, now working cooperatively with digital circuits, and sometimes doing entirely new power handling functions.

This course is intended to equip students with knowledge of fundamental electronics that will be important to a variety of pursuits in the field of electrical engineering, ranging from communications to power handling. Our emphasis will be on systems, and applications.

There are two fundamental topics that this class revolves around: Frequency response and feedback. A secondary emphasis is on power handling. Frequency response requires a background in calculus. We will be routinely using Laplace Transform techniques to represent what is going on in circuits. In a straightforward circuit lacking overall feedback, you need to understand the relationship between a transfer function representation of what the circuit does, a graphical representation (Bode Plot) of the frequency response, and the physical capacitors and other AC components of the circuit. For such a circuit, you can point to a particular capacitor, say, and then point to an inflection point in the graph and a term in the transfer function, that are the manifestations of what that capacitor does. Feedback makes things more complicated. This is where dependent sources covered in EE211 come into play, in “two port” representations of components. We will cover feedback a bit more formally and comprehensively than the textbook supports. Power handling is something we will see primarily in the laboratory.

This offering of EE252 features the same book that you had last semester. We can’t cover everything left in the book. We will have to be selective. It is assumed that you have background from EE251 in the design and analysis of single stage transistor amplifiers, both MOS and bipolar. You should be able to understand and do design and calculations concerning bias, gain, and input and output impedance. You should also be familiar with some fundamental two transistor circuits such as the differential amplifier, cascode amplifier, and the use of a common collector output stage.

We will spend more time with bipolar devices because that’s what we are using in the lab, and that’s the more difficult problem, even though for IC’s MOS is now more common. (However, this year I will be trying to get more MOS use into the lab, perhaps even for the power amplifiers. Beware: they are very sensitive to static, which is one reason we have in the past used bipolar. The other reason is that bipolar design is generally more challenging. If you can do bipolar, MOSFET’s are easier.)

Schedule: A planned schedule listing reading assignments and topics to be covered is listed below. The schedule is tentative with respect to the dates on which topics are covered.

Week of:	Topics covered	Reading, Tests
1 Aug 28	Overview, An example, the FM radio receiver	
2 Sept 6*	Amplification, Cascode and Differential amplifiers review	Chapters 4, 6 review
3 Sept 11	Frequency response	Chapter 7
4 Sept 18	Frequency response (continued)	Chapter 7
5 Sept 25	Power amplifiers (preview)	Notes, handouts
6 Oct 2	Frequency response (continued)	Chapters 7, 11 test#1
7 Oct 9*	Frequency response of Multistage amplifiers	Chapters 7, 11
8 Oct 16	Output amplifiers	Notes, handouts
9 Oct 23	Coupling, Frequency response for Multistage amplifiers	Chapters 11, 12
10 Oct 30	Operational-Amplifiers (selected topics)	Chapters 9, 13, 14
11 Nov 6	Feedback: Two port networks	Chapter 12, notes
12 Nov 13	Feedback	Chapter 12 test #2
14 Nov 20*	Feedback, stability	Chapters 12, 13, 14, 15
15 Nov 27	Feedback, stability, oscillators	Chapters 12, 13, 14, 15
16 Dec 4	Special circuit components: SCR's, Triacs, other odd stuff	handouts
17 Dec 11*	Review	
18	Exam	(comprehensive)

* indicates a "short" week with only one or two class meetings.

About the text and readings: This is a thick (and heavy!) book. We cannot cover everything of interest; we must be selective. I will be picking out particular parts of the chapters listed for the readings that we will emphasize. You should give a quick read of other sections so that you at least know what they are about, but we will not spend any time on covering those topics except perhaps in very summary manner.

Laboratory Exercises:

The planned laboratory schedule is shown below.

Laboratory Exercises (Dates are given for Wednesday lab session.)

Lab 0	Aug 28, 30	Common Emitter review lab (ungraded) – Be sure to bring your lab kit!
Lab 1	Sept 6, 11	Common Source review lab – Form report, due at end of lab period**
Lab 2	Sept 13, 18	Common Emitter amplifier - Formal Lab report due next week
Lab 3	Sept 20, 25	Common Source Amplifier – Formal Lab report due next week
Lab 4	Sept 27, Oct 2	Common Base, Common collector - Informal report due next week
Lab 5	Oct 4, 9	Differential Amplifier – Informal report due next week
Lab 6	Oct 11, 16	Class A, B, and AB power amplifier - Form report. Turn in next week
Lab 7	Oct 18, 23	Multistage amplifier – Formal report due 2 weeks from start in lab
Lab 8	Oct 25, 30	Power Amplifier – Formal report due 2 weeks from start in lab
Lab 8	Nov 1, 6	Power Amplifier – Demonstrations of operation (Formal due next week)
Lab 9	Nov 8, 13	Active filter – Formal report due next week
Lab 10	Nov 15, 20	Feedback and stability – Formal report due next week
Lab 11	Nov 27, 29	Thyristor lab (yet to be distributed) – form report due a week later
	Dec 4, 6:	Make-up: We are likely to need an extra week somewhere or other.

(** Lab #1 This report will count toward class participation only, unless we miss a lab.)

The lab exercises will be done by partnerships of two students. Ideally, everyone will keep the same partner throughout the semester. If we have an odd number, that will have to be

adjusted. There are six formal lab reports for each partnership. Each partner will do three of them, with the pair swapping off for each pair. One of each of the students should do 2 and 3, for example. For the later lab exercises, numbers 7 and 8 are the "big" ones. One student should do each. That leaves 9 and 10; those should be split too.

In like manner, there are two informal reports, numbers 4 and 5. Each student is to do one of them. There are also three "form" reports to be handed in at the end of the lab period or at the beginning of the next lab period, as applicable. Students are both to contribute to those, and credit will be shared. Finally, there is a lab exercise which will not be graded, lab 0. I will probably allow the last lab to be done as a formal lab for anyone wishing to do so for greater credit.

Grading: Tests will cover all material through the previous week. Tests will generally be on the last day of the week listed, unless an announcement is made setting the date differently. Tests are open book. They are expected to be hard. You will not have time to open your book very much, and still complete the test. Be well prepared. The exam will be comprehensive, but will have the major emphasis on the later topics.

There will be several homework assignments. The intent is to give you some practice on meaningful problems. Homework solutions will be distributed at the beginning of the class when the assignments are due. These assignments will be ungraded, but I will take them up to see how students have done. After discussion, there may be a pop quiz that covers some aspect of the homework material. (That will be on the day due or the following class.)

Grading Allocation:

2 tests at 18% each :	36%	up to 3 pop quizzes, total of	6%
class participation (HW? attend? Lab1)	4%	Three informal/form reports,2% each	6%
3 formal lab reports (per student)@6%	18%	Final examination:	30%

There will be an emphasis on good formal lab reports. Unacceptable reports will be stamped "Rejected," and returned with a grade of zero pending a required resubmission within a week. Resubmitted lab reports that pass only after being unacceptable will be penalized for the initial submission being unacceptable, probably by 10 points, possibly more in extreme cases. Resubmitted lab reports must include a reworked draft, a certification that you have taken the reworked draft to the Writing Center for help, which should also be evident in the annotations made on the draft. Then, the final reworked paper is then to be resubmitted along with the original rejected report, the reworked and annotated draft, and the Writing Center certification. (This is a lot of extra work, so, do it well the first time!) Lab reports that are acceptable may also be resubmitted with corrections within a week and will be given the average of the two grades. In such cases use of the writing center is not required. Resubmit the revised and original reports.

One issue that has led to problems in the past is a misunderstanding of just what should be in a laboratory report. Some students have thought that the report just describes and reports what was done in the lab. That is not the case in this course. A "lab exercise" is actually much more involved, including the design of a circuit, simulating and characterizing it, and perhaps modifying the design to meet specifications. All that happens before you enter the lab. If you show up for lab without this being done, you will fail the lab. (I will usually come by to check out each student team's preparation at the beginning of the lab period.) Then, in the lab, you build the circuit that you have designed and simulated, and see how it performs. You may need to make additional modifications (and simulate them). Finally, in the report, you describe the design process in detail, compare the design as analytically characterized to the specifications,

and then compare the design and specifications to the simulated design, and the actual circuit as built. We want design, simulated, and as built then compared to the specifications. We can then reach conclusions about how well it did, why, and what might be done differently. Your lab report covers all of this. Including graphs from PSpice, tables of results, circuit schematics and such, a good formal lab report will be on the order of 20 pages. Often the better lab reports will be the shorter, more concise ones. Longer ones where students have thrown in lots of BS (typically lots of theory or background) for padding usually grade lower. Sometimes the circuit as built will not meet the specs! Reasons can be varied, for example component values may be off a bit. When you see this happen, it is your responsibility to try and explain why. Don't just guess. Do some analysis. Not meeting spec in the lab is not necessarily a reason for a lowered grade. Being able to explain what happened is much more important. So, as you can see, lab reports for this course are pretty involved. Reports running up to 30 pages are not uncommon. Se the *Engineering Laboratory Reports Manual* for guidance on laboratory reports.

Each student in a pair will do half of the formal and informal reports, but is expected to get help from the other partner in helping do the lab exercise, collect data, and (very important!) review the report before handing it in. If a report shows lack of a good review (e.g. stuff missing, lousy organization, lots of format or spelling errors, or a grade below 70), the partner will be hit for -10% of grade value unless there is testimony that he did not get it at least a day in advance of it being turned in to review it, or the originating student did not make the corrections given, in which case the -10% hits the student turning in the lab instead. For an excellent formal report that received review, the reviewing student will receive a bonus (up to 10%). For formal and informal lab reports, provide a space for the student turning it in to sign as originator, and the partner to sign as reviewer. (If it was not reviewed, the reviewer should not sign, and let me know why.) If there is a problem, be sure I know. The form reports are submitted as one report by the partners at the end of the lab period, and the grade applies to both.

All material will be graded on a basis of 0-100, with most graded material allowing for grades higher than 100 with bonus questions (usually up to 10% extra) considered. On tests and the examination some questions may be "compensated" if large numbers of students miss them (indicating possibly a badly posed question or inadequate coverage of the topic in class). On such questions, some proportion of the "lost" credit will be returned. This is the only form of "curving" of grades in the course. All written work is expected to be neat and well presented. A penalty of up to 10% will be assessed for poor presentation, and in extreme cases, perhaps more.

The grades from all work will be weighted as given in the above table, totaled, and converted into the Wilkes 4.0 scale grading system using the following conversion:

93+:	4.0	83-87:	3.0	70-76:	2.0	60-64:	1.0
88-92:	3.5	77-82:	2.5	65-69:	1.5	below 60:	0.0

Since the homework assignments are not graded, you may receive help on these or even work with another student. However, if you do this, please indicate the degree of your own involvement. If you simply submit a xerox copy of another student's work, explain your own role in doing the assignment, which should not be limited to just operating the copier. The degree to which students participate in doing homework will be subjectively judged and may influence the final grade by up to a point in either direction in borderline cases, as well as affecting the subjective "class participation" part of the grade. The intent here is to allow any

degree of cooperation and help on the homework, and use the pop quizzes as the grading mechanism to motivate doing homework. A pop quiz is most likely to be given on the day that a homework assignment is due, or the following class.

The "class participation" grade will also suffer a deduction if your lab station is not properly cleaned up at the end of your work. Don't borrow or lend cables or leads, and put them back if you do so anyway! Be sure to clean up debris. Leave the multimeter with alligator leads connected, and the 'scope Channel 1 connected to the signal generator with a T connector. In addition, 1% of the 4% class participation grade is lost if you do not email me before the last class of the first week that you have read the syllabus.

Important: You MUST do every laboratory exercise. Even if your partner is the one submitting the report, you MUST be present and participate in the laboratory exercise. If you miss it, you must make it up, possibly without getting help from your partner if he is unavailable. (If your partner is doing the report, you must at least build and demonstrate and present the data informally when making up the laboratory exercise.) If you have not done or made up for all of the laboratory exercises, you will receive a FAILING grade unless there are extenuating circumstances that merit consideration.

Notes: I expect to have notes for the course that will be available as reserve material in the library to students who want to see them. I do not guarantee that my notes will match the lectures, since I do tend to depart from prepared notes on occasion, and often skip topics that I decide not to cover in class due to time limitations. A loose-leaf notebook of these class notes will be kept in the library on reserve. This will include some of the lecture materials or handouts used, worked homework assignments, and test solutions. You are not obligated to copy any of this; it is merely meant to be helpful. Any material that is really needed will be distributed in the form of handouts in class. Notes from earlier books used in the course are also included, and copies of earlier textbooks will be made available if requested. Sometimes it helps to see material described by a different writer.

About PSpice (or LTSpice): Spice is a very useful circuit simulation program. There are several varieties, including LTSpice and Cadence/ORCAD/Pspice. My tutorial material uses PSpice. You will be expected to use PSpice (or LTSpice) as an essential analytic tool, and you should have gained proficiency doing so in EE251. The Tront book, which is optional, is a valuable resource. It does have a copy of PSpice on CD ROM, but you might want to get a more recent version. The "Student version" should be sufficient for our needs. Be aware that if you develop a circuit with the student version, you can open it in the Professional version, but not the reverse. So, you might even want to run the student version (or, the "unregistered" version) in the lab. For our purposes, the one big advantage of the professional version is that it has more parts. So many more it is hard to find what you want. One of the biggest pitfalls in using PSpice version in the lab is that, even for some things as simple as a ground connection, there are 800 different parts, and only four of them do what you want (in the demo / unregistered version). OK, that may be an exaggeration. Maybe only one works. (Hint: use the components in the DEMO library.) This is where Tront can be very useful. The Ground and V sources are particularly tricky. When doing transient analysis, use VSIN. For AC (frequency sweep) use VAC. You have to change the circuit depending on what you are doing.

The Tront Book is now a bit dated, and the CD is an old version of PSpice. It's still useful, and it's available used for a reasonably low price. (I saw it at $8.50 on Amazon.) There

are differences in the more recent versions of Cadence ORCAD/PSpice. But, I find the book still very useful.

You may choose to use LTSpice instead. I believe you used that in EE251. It does have some advantages (e.g. price, availability for Mac, simplicity). Be aware, though, that Cadence ORCAD/PSpice is more of an industry standard; you might be expected during interviews to have some familiarity with it. Best of all, be proficient with both!

I am expecting to use ORCAD/PSpice for my examples and tutorials.

More about the Lab: As you know, there is no EE251 lab. The laboratory work that would complement EE251 is now necessarily part of EE252. However, many of the basic EE251 circuits were also covered in EE211 and EE283 and EGR222, though not in the depth and with the analytic rigor that we would really like. So, we will start with a Common Emitter and Common Source amplifiers, but include examination of frequency issues, which is covered at the beginning of EE252 anyway. The lecture material will coordinate with the lab. The lab exercises have been explicitly chosen to complement what we will be doing in the course. In some cases, your course homework assignment will be the design, PSpice modeling, and simulation and analysis of circuits you will later build, test, and analyze in the lab. The details of the lab exercises are appended to this syllabus. There may be some changes or adjustments. The last lab is not included.

If we have an odd number of students, for each lab one group will have to have three students. After the first formal lab, we will move one of those three to a different group. Then the same after the second formal. Maybe again later. Nobody has to move more than once to be fair, but that does mean you won't necessarily have the same partner throughout the course.

Paper copies of the Engineering Laboratory Reports Manual will be provided. The same material is available at < http://www.jbgilmer.com/LabManual/LabManual.htm >

Notice that at the end of the syllabus there are some documents that you will want to refer to in doing some of the lab preparation.

Course Web Site:

Material relevant to this course will be posted at my web site: < http://www.jbgilmer.com/EE252/EE252.htm >. Most of the materials there will also be available in paper form. Also see: < http://www.jbgilmer.com/EE252L/EE252L.htm >

Lab #0 First Week of Classes! Common Emitter Review:

The first (zeroth?) lab exercise is a review, and will not be graded (except as a portion of the class participation grade component). You are (before coming to lab) to design a single transistor, common emitter amplifier. It is to have an input impedance of at least 10K Ohms. It is to drive a load of a 15K resistor to ground. It is to be an AC amplifier, tested at the frequency of 10 KHz, with a 10 mV input signal. You are to use a power supply voltage no higher than 12V. Achieve as much gain as you can while building a well-designed circuit.

I'd like for each team's design to be different; I suggest you choose an "odd" value (unlikely to be the same as anyone else's) for the Collector resistor. Test your design with PSPICE before you come to lab. Have the schematic, DC (Q point) and transient results for 10KHz on paper, as well as your supporting design calculations and schematic. When you get to lab, build it and experimentally determine the actual gain. (Also, find the Beta of your transistor at the Q point chosen.) The whole point is just to get back into practice and remember how to do this stuff we had gotten to by the end of EE251, and see it work in the lab.

Be sure to bring your kit! Also, be sure you know who your partner is; you should figure that out ASAP.

Please note the handouts at the back of this syllabus. One of them discusses input impedance.

Lab #1 Common Source Review:

This lab exercise is also an EE251 review, and will be graded as a portion of the class participation grade component or, if we lose an informal/form lab, as a form report. You are (before coming to lab) to design a single transistor, common source amplifier using the 2N7000 MOSFET transistor. (Be sure to look up a data sheet.) It is to have an input impedance of at least 10K Ohms. It is to drive a load of a 15K resistor to ground. It is to be an AC amplifier, tested at the frequency of 10 KHz, with a 10 mV input signal. You are to use a power supply voltage no higher than 12V. Achieve as much gain as you can while building a well-designed circuit. (In other words, we have the same spec as Lab #0, except we are using MOSFET instead of bipolar.)

Use the same resistor value for the Drain resistor as for the Collector resistor in Lab #0. Test your design with PSPICE before you come to lab. Have the schematic, DC (Q point) and transient results for 10KHz on paper, as well as your supporting design calculations and schematic. When you get to lab, build it and experimentally determine the actual gain. (Also, find the transistor transconductance at the Q point chosen.)

Form Report:
Put on a page or few (along with names, section, station date):
1) The schematic
2) Bias and gain design calculations (showing how you designed the circuit)
3) Sketch input and output waveforms at 10 KHz as a properly annotated graph
4) Calculate the gain from lab observations, and compare to design, simulation results
5) Calculate input impedance
6) Calculate transistor transconductance from lab results.
7) Append simulation DC and AC transient response results.

EE252 Electronics 2 Laboratory Exercise #2
Common Emitter Amplifier

2.0 Objectives:

Understand basic amplifier circuits using bipolar transistors. Examine design tradeoffs concerning bias and quiescent point choices and input and output impedances, including issues of gain and clipping. Also, we wish to measure transistor AC base (r_π) resistance and compare it to the value derived from the diode equation. Most of the material covered in this lab should be familiar from EE251.

2.1 Pre-Lab assignment

Read the material in the book about bipolar transistors and common emitter amplifiers. We will be using the PN2222 as a common emitter amplifier. Figure 1 shows the overall circuit that we will get to.

The first part of the preliminary work is to design the bias network that establishes our Q-point. Assume that we will follow the "rule-of-thumb" the textbook gives of making V_C = 2/3 of V_{CC} and V_E = 1/3 of V_{CC}, which we will set at 12 Volts. Now we assume a Q-point Collector current. Pick a current between about 1mA and about 5mA. (If you are at the lab station nearest the door, use ½ mA, give or take 30% or so. At the next station back, use 1mA. The third one, 2mA. On the window side of the lab, use 3, 4, and 5mA, front to back. If we use another station, it would use 6mA.) Because the beta of this transistor is high, emitter current is about the same as collector current; you can use the same value resistor for both R_E and R_C. Decide on the value and then recalculate what I_C will be. Now calculate I_B . The PN2222 should have a beta between 100 and 300. Assume 200. To assure stability, the current through R_{B2} should be about 10 times I_B. Pick I_{B2} and I_{B1} to make the base about .7 Volts above the emitter. If you need a resistor value that you do not have, let me know.

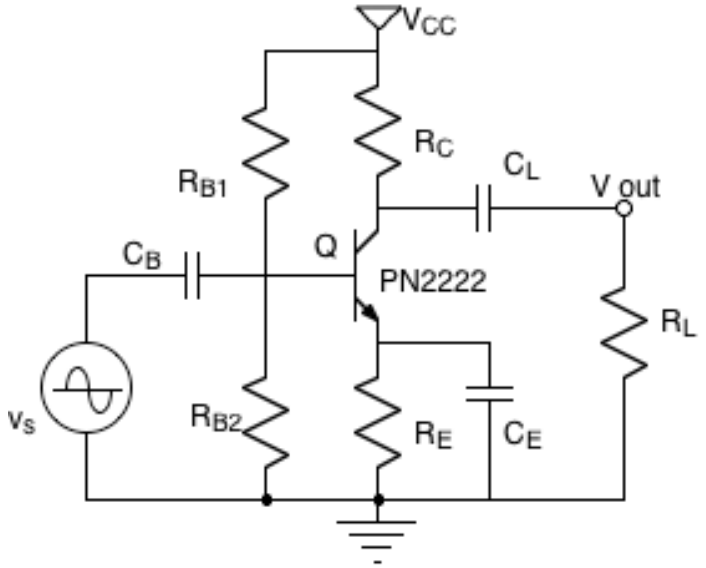


Figure 1 Common Emitter Amplifier

Now we would like to predict the AC “midband” performance. We will make C_E, C_B, and C_L "large" so that they do not affect the AC performance of the circuit. (Use a 470 μF capacitors for C_E and something around 10 μF for C_B and C_L.) Note that C_E shorts the emitter

to ground for AC, and C_B directly connects our signal source. Since the Base-Emitter junction is basically a diode, we can estimate its AC resistance as about .026V/ I_B. (You will recognize V_T there.) Now we should be able to calculate the input impedance, and the AC gain we will have with no load (R_L= infinite), and then with a load of 1K Ohms connected by C_L. Then, see if you can predict what the gain would be without having C_E in the circuit. Try the circuit in PSpice (at 1KHz), and check your bias and gain calculations. You should try out all of the things we will be doing in the lab with PSpice ahead of time, including the frequency sweep.

2.3 Build and check bias network

Construct the transistor and bias network (omitting any capacitors) part of the circuit shown in Figure 1, using the component values you calculated earlier. Power it up, and check the Q-point. Record the voltages and currents. If what you see is way off, there's an error, or you may need to adjust the resistor values to get at least close to the desired values. (And, go back and check your work!)

2.4 Complete the amplifier and Measure AC performance

Add the remaining components, except for R_L. Use your 470 μF capacitor for C_E and something around 10 μF for C_B and C_L. (Remember, they are polarized; be sure that the positive end is where it ought to be! Look at your bias circuit and simulation DC Voltages.) Connect the signal generator to the input, and use the oscilloscope to watch both the input and output voltages. (You may need to use a potentiometer or other Voltage divider to reduce the input Voltage to a small enough value to avoid clipping, since the signal generator doesn't go below 10-20mV!) Vary the input voltage magnitude and watch what happens to the output. Find the value of input and output that gives "clipping" (the output is no longer sinusoidal). Go to a voltage well below that, and record input and output magnitudes. Then figure the AC gain. Now yank out C_E and see if it makes a difference. Record the AC gain for that condition. (You may need to crank up the input signal to make the output measurable.) Now add a load of 1KΩ (remember to include a C_L coupling capacitor of perhaps 10μF as well as C_E!) and see what happens to your performance. Make the necessary measurements, and calculate both Voltage gain and Current gain. Also, calculate r_Π, the base-emitter diode AC resistance. Note that you will have to measure the input AC current to do this.

2.5 Frequency Response:

With the load of 1K Ohms, find the frequency response (magnitude and phase) for frequencies from 10Hz to 1MHz. Use at least two points per decade (10, 30, 100, 300,…). Derive a Bode Plot for your report, and compare to the simulation equivalent (need a VAC and a frequency sweep analysis in PSpice to do that.)

2.6 Report:

Report your results formally. Include your design process. Be sure your schematic is properly drawn and annotated. Compare the results you got in the lab with the results from PSpice as well as what you might expect from circuit theory models of the devices based on the diode equation for rπ and other models in the book. You may find it desirable to re-run PSpice with values adjusted to what you actually did in the lab, and include cases you may not have earlier if necessary to understand and explain your results. For frequency response, include an analysis and Bode plot based on your design as well as the simulation and lab results. The report is due one week after the lab work. (Refer to the Engineering Lab Reports Manual.)

EE251 Electronics 2 Laboratory Exercise #3
Common Source Amplifier and Frequency Response

3.0 Objectives:

Understand basic amplifier circuits using MOS transistors. Examine design tradeoffs concerning bias and quiescent point choices and look at frequency response. This lab is similar to the previous one, except using an MOS instead of a bipolar transistor.

3.1 Pre-Lab assignment

Read the material in the book about bipolar transistors and common source amplifiers. We will be using the 2N7000 NMOSFET.

The first part of the preliminary work is to design the bias network. Assume that we will follow the "rule-of-thumb" the textbook gives of making V_D = 2/3 of V_{DD} and V_S = 1/3 of V_{DD}, which we will set at 12 Volts. Assume a Q-point Collector current between about 1/2mA and about 5mA. (Use the same values as for the earlier bipolar lab #2.) Choose standard resistor values, and then recalculate what I_D should be.

Predict the AC performance. First make C_S, C_G, and C_L "large" so that they do not affect the AC performance of the circuit. (470uF for C_S and 100uF for the others should do it.) Note that C_S shorts the source to ground for AC, and C_G directly connects our signal source. Calculate the input. Predict what the gain should be. Try the circuit in PSpice, and check your bias and gain calculations.

Choose input and output capacitors to give about 10 Hz and 100 Hz poles for those capacitors, respectively. (The RC time constant should correspond to 1/ω for those frequencies.) Use a 1K Ohm load, and put a 1K Ohm source resistance between the signal generator and your circuit. Use the “large” (470uF) capacitor for Cs. Model it with PSpice and see if you get “cut off” (rolloff of .71 in Voltage) at the 100 Hz frequency as expected. (In Pspice, use the MbreakN model with parameters for the 2N7000, if you do not find the 2N7000 part.) Get a Bode plot for your PSpice model. Bring your results to lab.

3.2 Build and check bias network

Construct the transistor and bias network part of the circuit, using the component values you calculated earlier. Power it up, and check the Q-point. Record the voltages and currents. If what you see is way off, adjust the resistor values to get at least close to the desired values.

3.3 Complete the amplifier and Measure AC (midband) performance

Add the remaining components, including R_L. Use “big” capacitors for C_S and C_B. Connect the signal generator to the input, and use the oscilloscope (at 1KHz) to watch both the input and output voltages. Vary the input voltage magnitude and watch what happens to the output. Find the value of input and output that gives "clipping" (the output is no longer sinusoidal). Go to a voltage well below that, and record input and output magnitudes. Then determine the AC gain, and record it. Calculate the Current gain as well.

3.4 Frequency response: Use the 10Hz and 100Hz capacitors for C_S and C_L. Sweep the frequency of the signal generator from 10 Hz up to 1 MHz, recording input and output amplitude and phase at each frequency, so that you will be able to generate a “Bode plot” of your actual amplifier’s response.

3.5 Report: Write a Formal report. Results should be comparable to that for Lab 2. You should compare design/theory vs PSpice modeling vs actual performance in the lab. Be sure to include anything “interesting” in your Conclusions.

EE252 Electronics 2 Laboratory Exercise #4
Common Base and Common Collector Amplifiers

4.0 Objectives:

Understand these basic amplifier circuits using bipolar transistors.

4.1 Pre-Lab assignment

Read the material in the book about bipolar transistors and common base, common collector, and differential amplifiers (signal in at v+, ground v-). We will be using the PN2222 as before, and the bias network for common base operation will be the same as for the earlier common emitter circuit. (Be sure to bring information on how you built the common emitter amplifier.) The common - base amplifier is very similar, except for the AC connections.

Analytically model the circuit and predict what the gain will be, both for the Common Base amplifier alone, and the combination with the Common Collector power amplifier added. Then model the circuits in PSpice and compare the results. Bring these results to the lab. Remember that the signal generator has a nonzero source resistance! Take it into account equivalently in both your analytic work and PSpice work. Be consistent in how you measure gain – from the actual amplifier input, or from the theoretic Thevenin ideal source. (You might want to wire up the circuits before coming to lab, and even test Q points.)

4.2 Build and characterize the common-base amplifier

Build a common base amplifier, as shown in Figure 1 below. Use the same resistor values (and Q point) as in the common emitter lab. Initially, treat Rs as zero. Use "large" capacitors - the big 470 and 1000 microfarad electrolytics in your lab kit should be big enough for C_E. Be sure you get the polarization correct! Write down the R and C values you use and the DC voltages measured at the Collector, Base, and Emitter (and the power supply voltage).

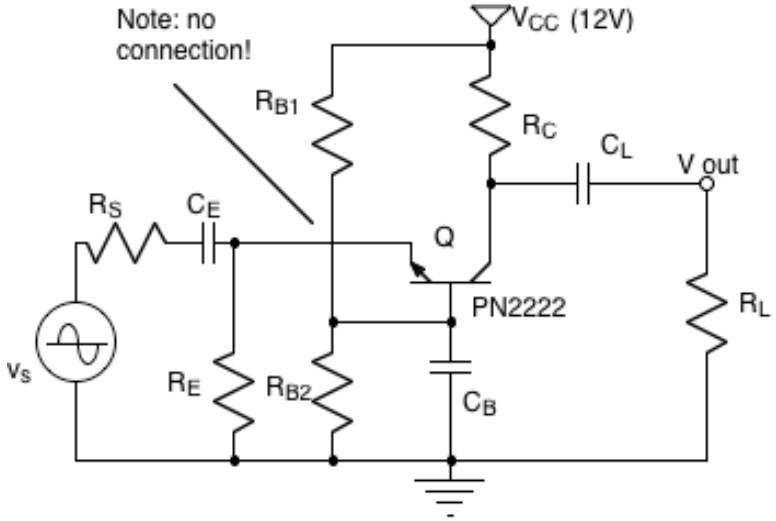


Figure 1: Common Base Amplifier

With the signal generator, inject an input voltage such that you do not get any significant clipping on the output, but try to use a large enough signal so that it is not swamped by noise. Use a sinusoid. Give the input AC (peak) voltage (measured at the circuit input). Sketch the output waveform. Now add a resistor Rs = 100 Ohms to the circuit. This makes an AC voltage divider at the front of your amplifier. The input voltage at the transistor emitter, and the output

voltage, should be reduced proportional to the voltage divider formed by Rs and the AC amplifier input impedance. You can now calculate the input impedance. Calculate the voltage gain and current gain.

4.3 Add a common collector output stage:

Add a common collector output stage, driving a 100 Ohm load. This circuit will substitute for the 1000 Ohm load used earlier. Figure 2 illustrates this. Use 100 Ohms for R_{E2} also. (Watch out for too much dissipation! Do you need more than 1/4W resistors for R_L and R_{E2}? How will you handle more power?) As a consequence of this different load, the common base amplifier (when considered alone) should have a different output voltage than before. Measure the AC voltage at the input to the amplifier (at C_E), at the first transistor collector, and at the load. You can then calculate the voltage and current gains of each stage. (The input current can be calculated from the voltage drop across Rs. The final output current can be calculated from voltage since R_L is known. The current into the base of Q2 (the CC stage) is more of a problem. Assume it is 1/Beta times the AC current through both R_{E2} and R_L. (Use your multimeter to estimate transistor Beta.)

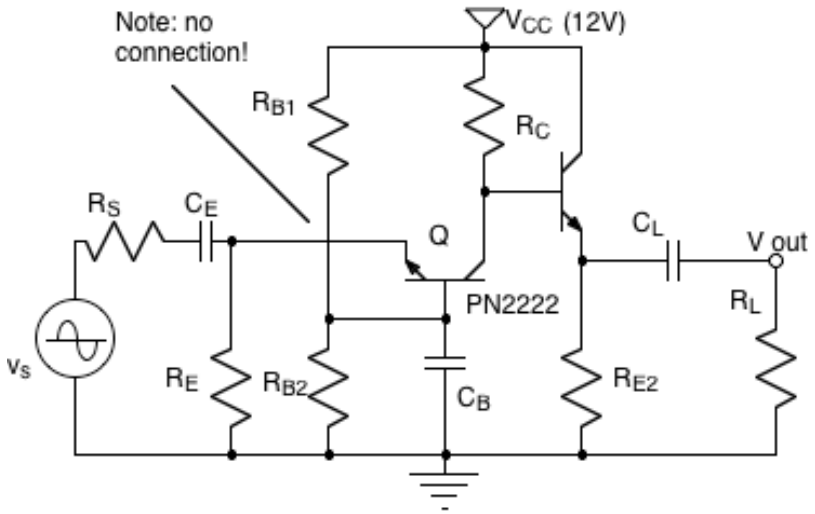


Figure 2: Cascaded Common Base and Common Collector Amplifiers

4.5 Extra:

Add frequency analysis to the exercise for extra credit. If you do this, include PSpice frequency amplitude plots and compare that to what you get for a frequency sweep in the lab. (We are particularly interested in differences between this and the differential and common emitter amplifiers at the high end.)

4.6 Report:

Make an informal report your results. Include written text only for abstract, conclusions. Skip Procedure. Include design work. Hand written design documents are OK. Include PSpice circuits (as built) showing Q points, and transient output plots showing how you calculated gain. Show how you calculated Rin and Rout for the CB amplifier from lab data. Lab Results and Comparisons between Design, PSpoice and lab Results in tabular form are fine. Include PSpice Bode plots and actual circuit plots (amplitude only) if you do the frequency stuff for extra credit, Be sure to include anything ”interesting” in Conclusions. We really are interested in two separate issues: How does adding the CC stage help the CB amplifier, and how do CE, CB, and CB+CC (all using the same load and I_C and most of the same component values) compare?

EE252 Electronics 2 Laboratory Exercise #5
Differential Amplifier

5.0 Objectives:

Understand the differential amplifier.

5.1 Pre-Lab assignment

Read the material in the book about differential amplifiers (we will use them "single ended", with signal in at v+, ground v-). We will be using the PN2222 as before. Design so that the bias conditions will be the same as for the earlier common emitter circuit. The Collector resistor (on the output side) should be the same as before. We will use two power supplies of +/- 6V so that we have the same power supply Voltage range (12 Volts) as before. We need a capacitor only for the output coupling to the load (of 1K Ohm). Calculate the capacitor for a low frequency cutoff at 100 Hz. A differential amplifier, used single ended, is equivalent to CC+CB.

Analytically model the circuit and predict what the gain will be at 1KHz. Then model the circuit in PSpice and compare the results. Do a frequency sweep from 10Hz to 1MHz. Bring these results to the lab. (You might want to wire up the circuit before lab.)

5.2 Build and characterize the amplifier at midband:

Build the differential amplifier. Use the same R_C value (and Q point currents) as in the common emitter lab. Initially use 100uF for C_L. Be sure you get the polarization correct! Write down the R and C values you use and the DC voltages measured at the Collector, Base, and Emitter of both transistors (and the power supply voltage).

With the signal generator, inject an input voltage at 1KHz such that you do not get any significant clipping on the output, but try to use a large enough signal so that it is not swamped by noise. Use a sinusoid. Give the input AC (peak) voltage (measured at the circuit input). Sketch the output waveform. Now add a resistor Rs = 1K Ohms to the circuit. This makes an AC voltage divider at the front of your amplifier. The input voltage at the transistor base, and the output voltage, should be reduced proportional to the voltage divider formed by Rs and the AC amplifier input impedance. You can now calculate the input impedance. Calculate the voltage gain and current gain.

5.3 Find common mode gain:

Now, instead of injecting the signal only at the positive input base (with the negative input grounded), inject the signal at both inputs. Crank up the amplitude to see if you can get a readable common mode output Voltage. Calculate the common mode rejection ratio.

5.4 Frequency Sweep (single ended input):

Perform a frequency sweep from 10 Hz to 1MHz. Compare what you get to the PSpice results. (We are particularly interested in differences between this and the differential and common emitter amplifiers at the high end.)

5.5 Report:

Make an informal report your results. Include written text only for abstract, conclusions. Skip Procedure. Include design work. Hand written design documents are OK. Include PSpice showing Q points and transient output plots showing how you calculated gain. Show frequency analysis. Lab Results and Comparisons between Design, PSpoice and lab Results in tabular form are fine. Include PSpice Bode plots and actual circuit plots. Be sure to include anything "interesting" in Conclusions.

EE252 Electronics 2 Lab #6
Power Amplifiers Introduction

6.0 Purpose:

This lab exercise is intended to prepare students for Lab 8, Design, Construction, and Characterization of a Push-Pull Audio Amplifier. Here we will look at certain key aspects of push-pull amplifier design in a relatively low power, low risk manner. In particular, we want to look at single ended versus push pull design, and also look at crossover distortion, biasing issues, and driver issues for push pull complementary output power amplifiers. The report is informal, made on the forms provided.

6.1 Preparation:

Take a quick skim of the "Output Stage" material in the text. Read the Horowitz and Hill and the RCA handbook material (handouts). Take a look at several audio amplifier designs, focusing particularly on the output (push-pull) circuits. Read this lab exercise description and come to lab prepared by calculating needed component values where necessary. Be sure to have TIP-31 and TIP-32 transistors and their heat sinks from the EGR222 Mechatronics lab kit. (You will need one of each. Unless you cause one to fail catastrophically and need to replace it.) Note: be careful with resistor values. For some you need more than ¼ Watt, and beware that some of the older ½ Watt resistors have anomalous, wrong values. Check with your meter.

6.2 Part 1: Single ended power amplifier:

Build the circuit below. Find R values to bias the power transistor so that with no signal, there is negligible DC current through the load. Record your circuit as built, Q-point data, and then try input signals of different amplitudes until you get clipping. Draw the waveforms for the signal just before clipping (you might see some distortion) and well into clipping. Plot output vs. input characteristics for this amplifier. (You should use the large "clipped" waveform and put the oscilloscope into Y vs. X mode to generate a nice graph.) Supply other data asked for. (Note that you need a non-polarized input capacitor. You can use polarized capacitors back – to – back. Design to pass signals at least as low as 400 Hz without significant distortion. R_E is chosen to give maximum power to the load.) Note: Some power resistors are available in the lab. You should use them if you need power handling, but please give them back later; they are expensive. Use a value close to what you calculate; you don't have to be exact.

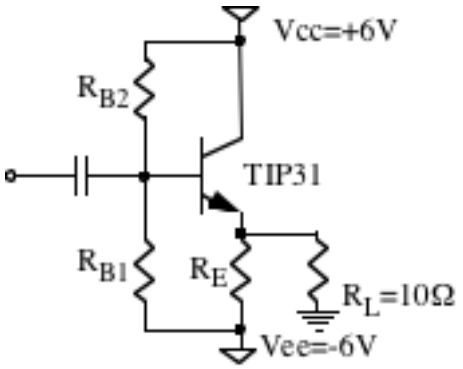


Figure 1 Single ended common collector power amplifier

6.3 Part 2: Push – Pull Class B power amplifier

Build the following circuit. Supply bias resistors having symmetric values, so that with no signal the Base Voltage is very close to zero. Now, try different signal sizes. See how large a signal you can amplify without clipping, and show clipped and non-clipped waveforms. Generate an output vs. input plot, and supply other data as asked for in the report section.

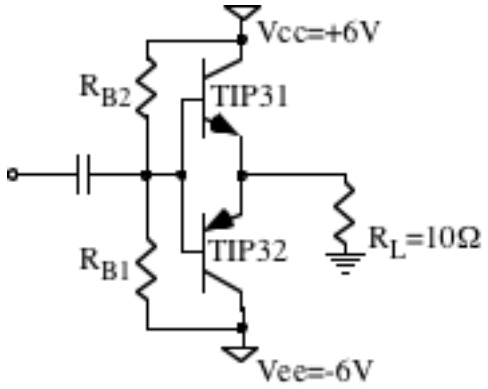


Figure 2 Class B Push – Pull Common collector power amplifier

6.4 Part 3: Experiments with bias conditions: Class AB amplifiers

Modify your Push-Pull amplifier to add some bias adjustments as shown in the figure below. Use a relatively small variable resistor for R_{B3}. (We should be able to obtain some 500 Ohm 5W pots before lab. If we have to, we can use 1K pots, but be sure to start out with a LOW overall resistance close to zero.) Use a small resistor of about an Ohm or ½ Ohm (Two one ohm resistors in parallel) for R_{E1} and R_{E2}. Use a meter to measure current through R_{E1} continuously while doing this part of the exercise, and immediately shut the power off if you see the DC current approaching an Ampere. If the resistors are ½ Watts rating, you don't want more than ½ Ampere. (If you can, set a current limit of 1A on the power supply.) Be sure to have heat sinks on the transistors. The point here is to watch what happens to distortion as the bias changes. Watch the input vs output curve and the DC current through RE1 as the resistance in RB3 increases. Find a spot (an RB3 resistance) where it looks like you have just eliminated the crossover distortion, but the DC current has not gone up very much. Plot the output waveform, and answer the other questions.

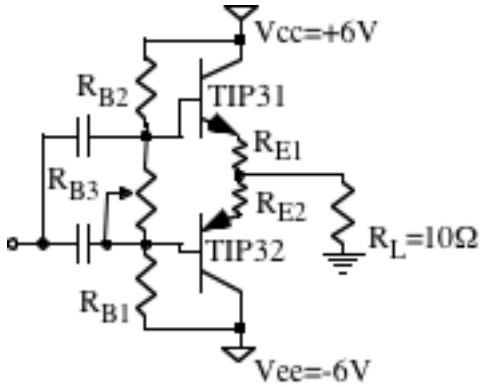


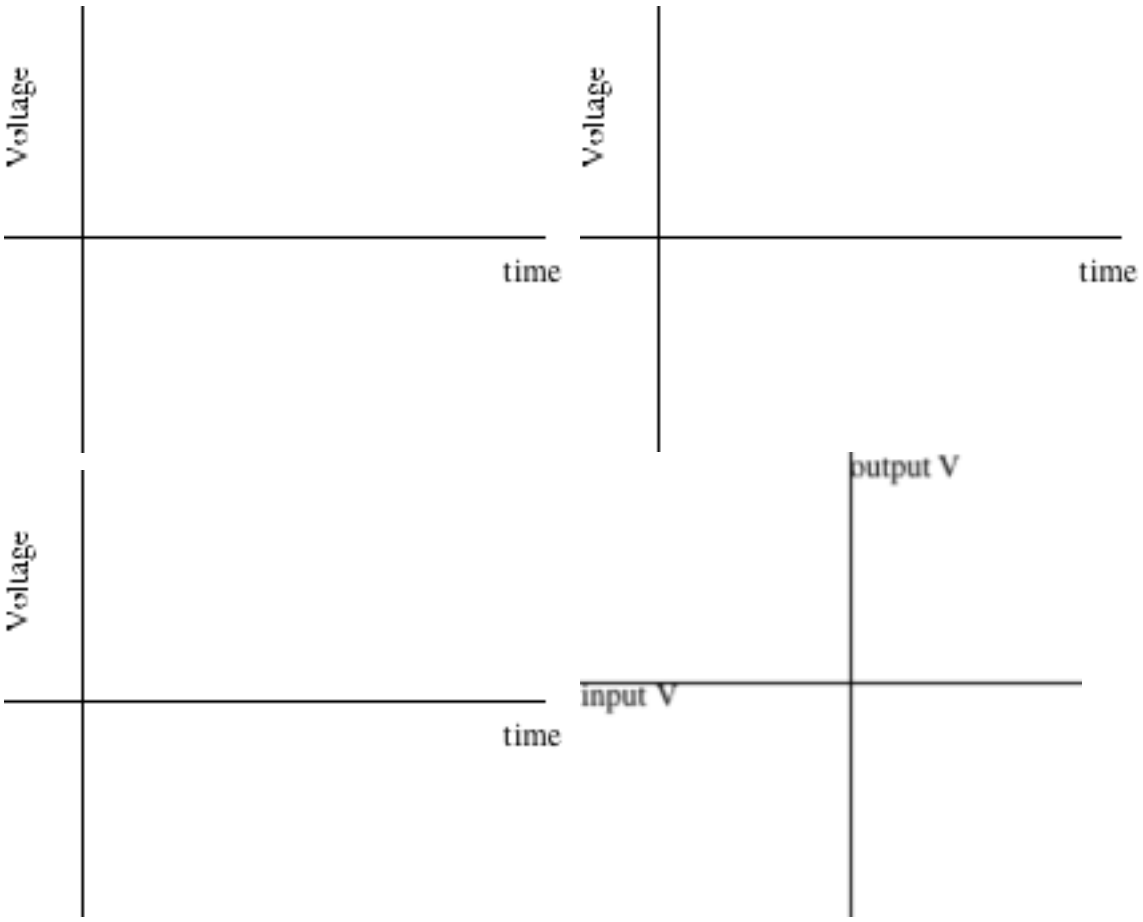
Figure 3 Class AB B Push – Pull Common collector power amplifier

6.5 Report: Fill in the data and accurately sketch and annotate the graphs on this form report: (Annotate your graphs properly. That's where most credit is lost on this lab!)

Lab Exercise #5 Power Amplifiers Introduction

6.2 Single ended amplifier Circuit (Be sure to include part numbers and component values.):

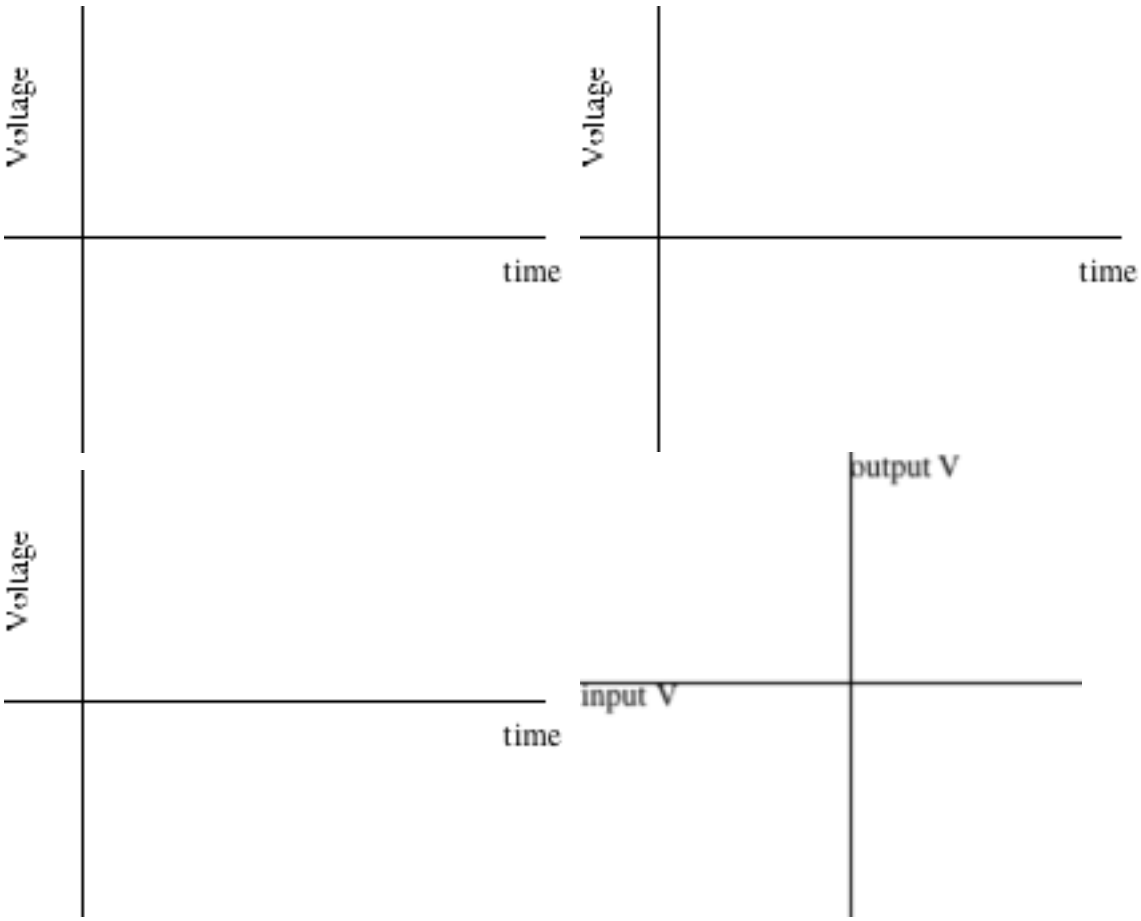
Waveforms (Give 3: small signal, just before clipping, and well into clipping. XY for well into



Largest (unclipped) AC power to load:_____ Efficiency:_____
(show calculations; append extra page if needed.)

6.3 Class B amplifier Circuit:

Waveforms (Give 3: small signal, just before clipping, and well into clipping. XY for well into)



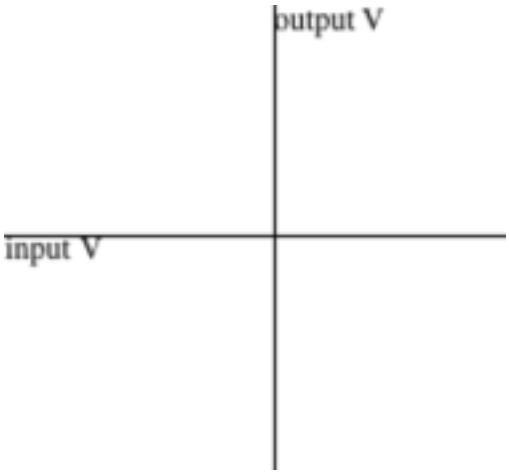
Largest (unclipped) AC power to load:_____ Efficiency:_____

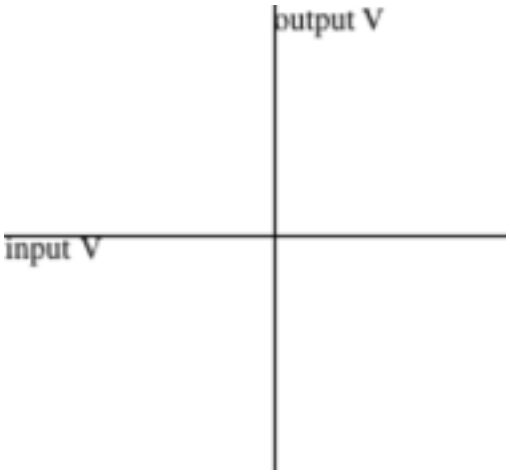
Signal Voltage (peak) below which output is negligible:_____

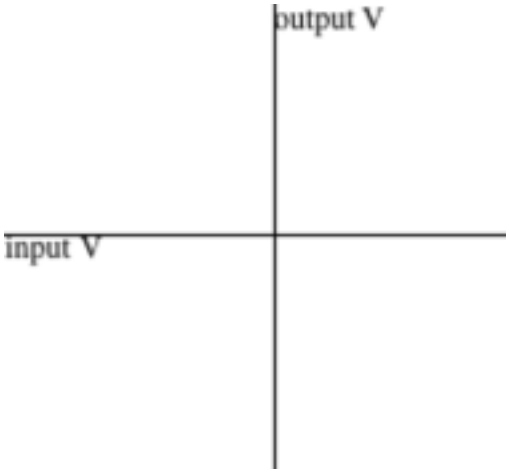
6.4 Class AB amplifier Circuit:

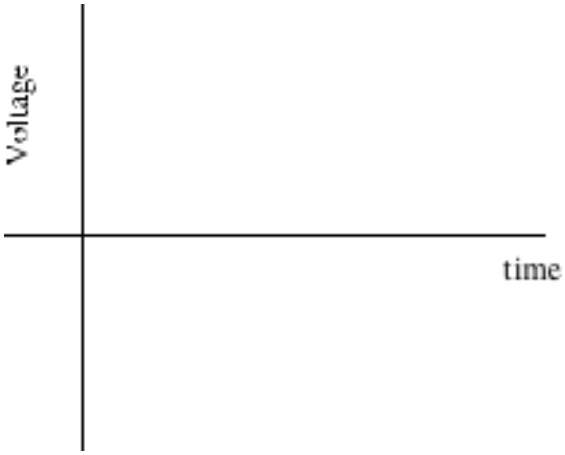
Waveforms (Give 3: out vs in for small signals with three different values of RB3, showing with crossover distortion, having just eliminated it, and well beyond. Show AC out at just beyond where you get significant crossover distortion.)

(For each I/O graph, identify the RB3 value, and zero signal collector current.)









Largest (unclipped) AC power to load:_____ Efficiency:_____

EE252 Electronics 2 Lab 7 Multitransistor Amplifier Design

(Note: this lab exercise may be changed a bit.)

7.0 Background:

In practical applications we usually need more amplification than one transistor alone can provide. An AM radio is a simple example of this. A superheterodyne radio includes (perhaps) an initial RF stage, a "mixer" where the original signal is mixed with the output of a local oscillator to give an IF frequency, then the IF is amplified to a level large enough to be rectified into an audio signal, which is then amplified enough to power a speaker. The power pulled out of the ether is very small, on the order of microwatts. But we need to drive an 8 Ohm speaker with perhaps several Watts. So, overall, we need 6+ orders of magnitude (>60 dB), and that does not account for losses in the mixer and demodulation. Figure 1 gives an overview of such a radio. (Sometimes broadcast AM radios omit the RF amplifier since signal levels are high.)

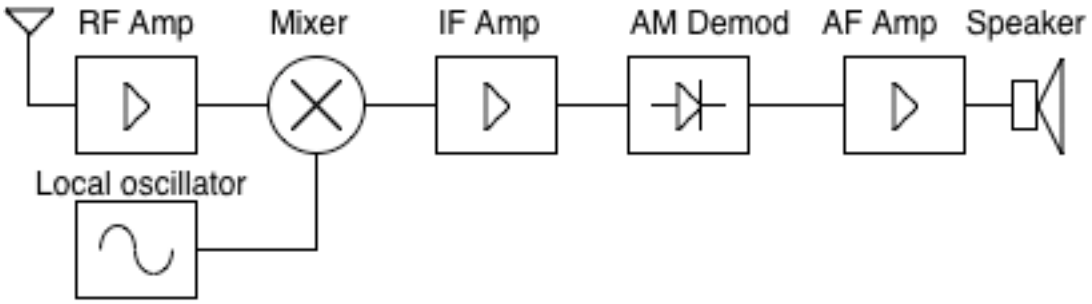


Figure 1 System Overview

For the RF and IF amplifiers, we not only need gain, but we need for that gain to be effective in the relatively high frequencies of interest. For broadcast band AM radio, this is no longer particularly challenging, since the frequencies are about 550 KHz to 1.6 MHz (RF) and 455 KHz (IF). FM receivers operate with RF around 100 MHz and IF of 10.7 MHz, and TV has frequencies up towards a GHz, and about 40 MHz for IF. In general, frequencies that engineers must deal with are increasing, and attention needs to be given to the limitations of the devices (transistors) and how those limitations can be mitigated.

In this lab, we will focus on frequency performance of a multitransistor amplifier such as that used in an IF unit, without yet concerning ourselves with the filtering function of typical RF and IF amplifiers. To simulate the effects that are seen at very high frequencies, we will "cripple" our transistors by artificially adding to the parasitic capacitance, that is, the capacitance between terminals, and in particular that from Base to Collector. Thus, we will be able to see the effects of such performance limits without needing to use inconveniently high frequencies.

Two different approaches will be examined. A cascade of common emitter amplifiers should offer the greatest gain, since this configuration amplifies both voltage and current. However, the negative feedback through the parasitic capacitance from collector to base tends to limit high frequency performance. The other approach is called a "Cascode" amplifier, which couples a low voltage gain common emitter transistor to a common base amplifier. We will add a third CC output stage like we did in lab 4. The desired voltage gain is achieved by the common base stage, in which the parasitic capacitance has a much smaller effect.

Note: this lab merges what was originally going to be two labs. It might be reasonable for each partner to develop one of the designs, then cross critique them. Or, I will assign one design approach or the other (cascade vs cascade) to different teams.

7.1 Specification:

We wish to achieve as much gain as possible, with as high a frequency performance as we can. We will use 10 KHz as the projected IF frequency we want to handle (10MHz would be more typical). We are allowed to use two (cascade) or three (cascade) transistors, and should be frugal in our use of other components as well. (No transformers or inductors!) We would like to achieve a voltage gain of 40 dB while driving a 1K Ohm load (the detector diode) and taking our signal from a source (the mixer) that has a 10K Ohm output impedance. We recognize that we may not achieve our gain goal, but if we cannot, the problem will be bucked up to management and perhaps we will then be allowed to add another transistor stage (but that is outside our current scope).

7.2 Preliminary work:

Design a two-stage common emitter amplifier. Attempt to meet the stated specification. To simulate the parasitic capacitance, add a .001 microFarad capacitor between the Base and Collector terminals of each transistor. (This is equivalent in effect to 1 picoFarad at 10 MHz.) Simulate the circuit in PSpice, and see if it reaches the goals. Note that you should select blocking and bypass capacitors so that 10 KHz is easily passed. Run a Bode plot to see how the amplifier performs. (We don't care about phase.)

Design a Cascode amplifier (with CC output) to do the same job. Add the same extra capacitors here too. Use PSpice to see how your design performs. We don't expect as much gain from this one. (But it uses direct coupling and fewer components, making up for the extra transistor.)

For both of these you will probably want to vary things like the selected operating points, R_C, R_E, and such to examine tradeoffs that might help. For the common emitter cascade design you should at first try it with emitters fully bypassed, and then maybe add some AC emitter resistance (at the sacrifice of some gain) to improve frequency performance.

7.3 Laboratory work:

Build both (or one?) amplifiers. Confirm that they work properly. Perform a frequency sweep with a sinusoid signal ranging in frequency from 100Hz up to 1 MHz to assess the performance of each design. (This is a good place to use LabView if you feel comfortable doing so.)

7.4 Analysis and Report:

Write a Formal report on what you have done. Include your design work where you calculated appropriate values and the expected gains and frequency responses. Because of the length of this report, you can put the design and design analysis in an appendix, and use neat hand drawn figures and formulas for that. It should still be well organized and presented. Include an analysis and discussion of actual versus simulated vs predicted performance, and reach a conclusion concerning which design should be utilized. Show your work neatly, well organized and presented, and justify your conclusions with your analysis. You should note anything unusual or interesting that you observe. (All that is really 'conclusions".) Lab Results and comparison of design vs simulation vs lab should be in tabular form to allow easy comparison. You may want to include recommendations for further refinements, if that is necessary or would add value. Include specifically whether the performance goals could be met, and what is recommended in order to meet them.

EE252 Electronics 2 Lab 8 Power Output Amplifier Design

8.0 Background:

An AM radio ultimately must deliver a signal to a speaker with enough power to be heard, or even to be "loud" for certain situations. A superheterodyne radio is shown in Figure 1. We need to drive an 8 Ohm speaker with perhaps several Watts. The audio amplifier must take a fairly weak signal at high impedance from the detector (demodulator) and amplify it enough to drive this low impedance load. This is usually done with early stages (the pre-amp) providing primarily voltage gain (and also volume and tone controls), and the power amplifier providing current gain. In order to drive the speaker efficiently while providing sufficient power at an acceptable cost, push-pull configurations are normally used for the last stage.

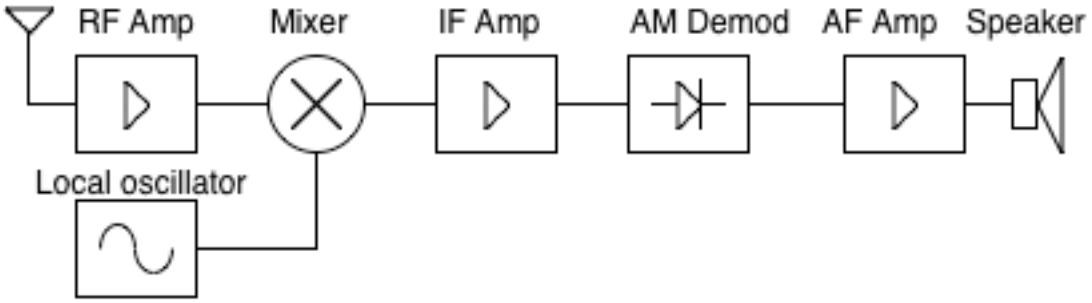


Figure 1 System Overview

Two different approaches can be considered. In the simplest, complementary common collector transistors are used, with direct coupling and a dual supply. Operation can be examined from Class B to Class AB, including the effects of distortion to find the “sweet spot” that gives minimal distortion without a large Q point current in the output stage. The second approach can vary, at the student team's choice: Use Common Emitter, both NPN, through a transformer, a quasi-complementary common collector approach, or some other scheme, perhaps even complementary common emitter without a transformer (for the truly adventurous).

8.1 Specification:

We wish to achieve as much gain as possible, and provide enough power so that the system can drive an 8 Ohm speaker with enough power to be obnoxious. The amplifier should provide several Watts to the load at signal peaks. It should pass frequencies from 100 Hz. to 10K Hz. The input from the AM demodulator is assumed to be about 200 mV at most. We would like an input impedance of about 1000 Ohms. Either a split or single power supply can be used, and the Voltage can be chosen as desired limited only by what is available and by the specifications of the transistors and the heat sinks to which they can be attached.

8.2 Preliminary work:

Design an output power amplifier. Your design should be different from others in the class. If it is too similar, I will have to ask someone to take a different approach. Provide a method for varying its operation from Class B to Class AB (by varying the Voltage offset between the output transistor bases). Simulate the circuit in PSpice, and see if it reaches the goals. Run a Bode plot in PSPICE to see how the amplifier performs. Do a phase plot as well to see whether we get significant shifts in the pass band. Examine the waveform and observe

distortion under conditions of peak power for which you have designed, and for 1/10 of peak power, for a mid-band frequency, say, 400Hz or 1KHz.

8.3 Laboratory work:

Build the selected amplifier. Perform a frequency sweep with a sinusoid signal ranging in frequency from 10 Hz up to 100 KHz to assess the performance of the amplifier. Determine distortion under the same conditions (full power and 1/10 power) for a mid-band frequency. Listen to the amplifier using pure tones and perhaps music of your choice, and make a qualitative assessment. Note that this is a 2-week lab. The degree of complexity is significantly beyond what you have done before. Constraint: No fair using an op-amp for the driver (V gain) stage.

8.4 Analysis and Report:

Write a report on what you have done, including an analysis of actual versus predicted performance, and reach a conclusion concerning which design should be utilized. Show your work, and justify your conclusions with your analysis. You should note anything unusual or interesting that you observe. You may want to include recommendations for further refinements, if that is necessary or would add value. This is to be a formal lab report.

8.5 Extra Credit Project Discussion (looking toward Lab infinity and beyond):

Eventually we would like to use these projects as parts of a radio receiver. We have some simple L and variable C components and an MK484 integrated circuit RF amplifier and detector that can be used to drive the amplifier to turn this project into an AM radio, as shown in Figure 2 below. This can pull in relatively strong AM stations. (Unless most of SLC is in the way!) A somewhat lesser quality amplifier can be made with two NPN transistors (much less gain) shown in Figure 3.

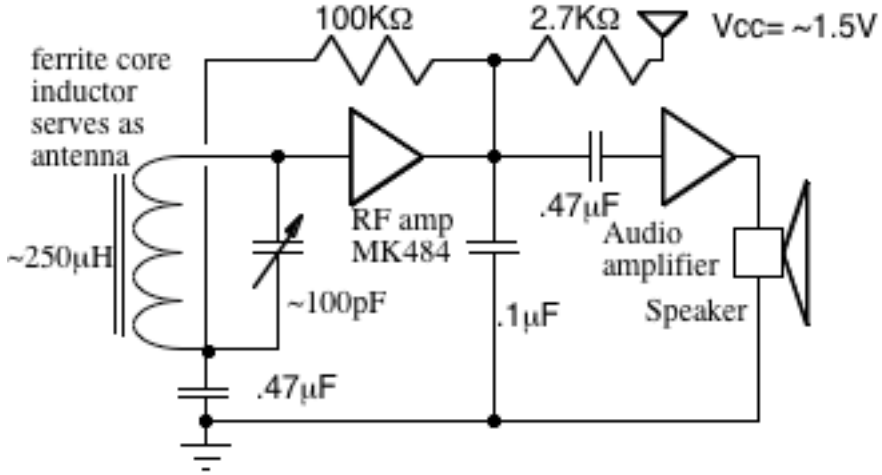


Figure 2 Simple Receiver based on MK484

Other possible approaches for an RF amplifier include a differential arrangement (common collector followed by common base, or cascode (common emitter followed by common base). In any case, a high input impedance is very desirable because the "Tank" circuit will only have a high Q if it is loaded only slightly. The use of a secondary winding often only a few loops compared to perhaps 100 or more for the primary, allows the tank circuit to drive a lower impedance source, as seen in Figure 4.

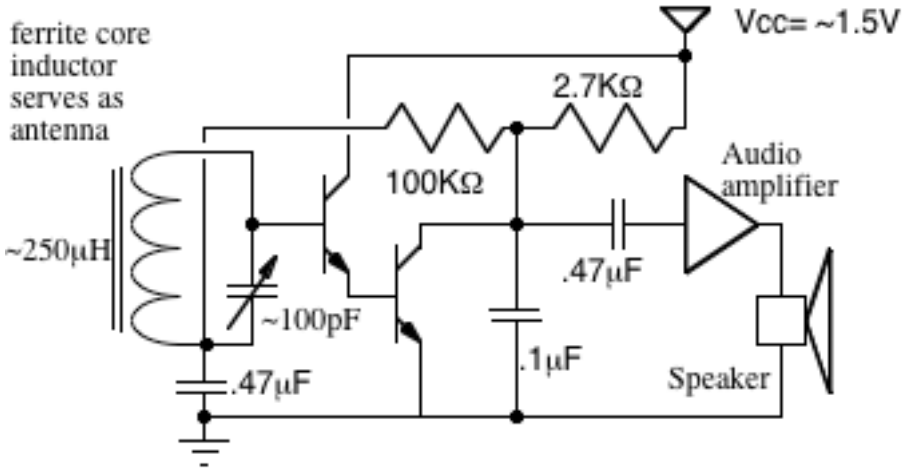


Figure 3: Simple Receiver with Common - Collector - Common Emitter RF pair

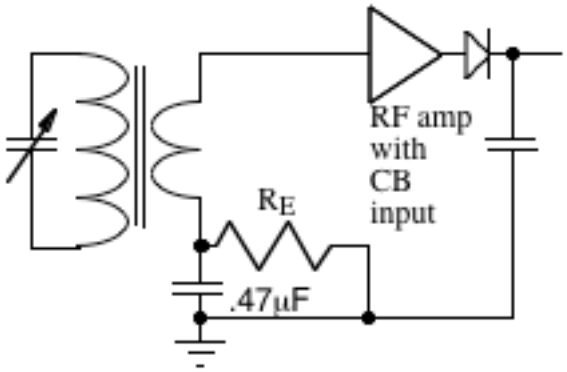


Figure 4

One important issue is how to do the tuning. Tuning capacitors are available as variable capacitors including sections of up to 160pF and 120 pF. We will get some. (The modern approach is to use Varactor diodes: A DC voltage across the diode determines its capacitance, and this is used to change the natural frequency of the tank circuit. The nonlinear characteristic of the diode is negligible because this method is only used at the front end where signals are very small.) Calibration and then selecting tuning voltage based on the desired frequency is an easy job for a microcontroller. Using a varactor diode would be an interesting "extra" for the AM radio project. But, we have so much to do that this is outside practicality in this course.

Another possibility is to implement a full superheterodyne receiver. This is more than we can accomplish in this course. In this case, tuning is needed for the first RF stage (which could be the cascode amplifier) and for an oscillator. The IF amplifier (using the common emitter cascade) is at a lower frequency, and can accommodate 2 or 3 tank circuits that do not need to be tuned as the station is changed. This gives superior selectivity. A diode can be used as a mixer, or (for greater efficiency) a more sophisticated multiplier. If varactor tuning is used, the calibration for the two diodes needs to be different, but in a production radio a microcontroller could handle that issue. (One could also use a broadband RF amplifier, but that risks mixing in two stations in different bands.)

Note: We may consider using power MOSFETs, or allow the use of them, for the output stage.

EE252 Electronics 2 Lab 9 Active Filter Design

9.0 Background:

The filter to be designed, built, and characterized in this lab exercise is part of a system that will digitize sounds to be recorded for automated responses for a robotic voice. The overall recording system is shown in Figure 1. This project concerns only the low pass filter. The sampling frequency to be used by the D/A converter is 8 KHz, the same frequency used in telephony. At that sampling rate, the maximum frequency that can be reproduced is 4 KHz, the "Nyquist Frequency." Frequencies above 4 KHz "alias" into lower frequencies, so that 5 KHz in the original audio signal would appear to be 3 KHz in the digitized signal, and 6 KHz would appear to be 2 KHz. We want our system to reproduce well audio signals of 1 Volt peak to peak having frequencies up to 2 KHz. That means that we need a low pass filter to get rid of signals above 2 KHz. From 2 KHz to 4 KHz is a "guard band" in which signals can be reproduced, but we will not try to do so at the mid-band amplitude. Beyond 4 KHz to 6 KHz signals should be low, but they will appear as 4 KHz to 2 KHz once digitized, and they can be suppressed further with digital signal processing after conversion. But above 6 KHz, signals will alias into our pass band. We are using an 8 bit A/D converter, so each bit is about 1 / 256 of the full range. If the 6KHz and above band is attenuated by a factor of 100, any signal that gets through is not much greater than the quantization noise. (We would really prefer a factor of 200 reduction.)

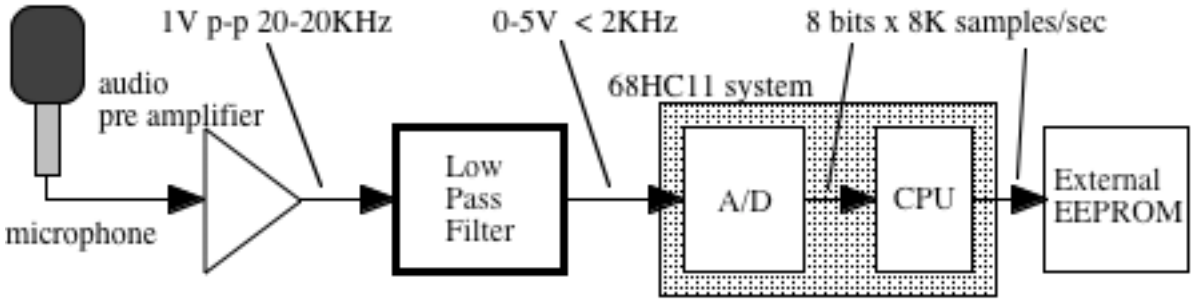


Figure 1 System Overview

9.1 Specification:

The Low Pass Filter design must accomplish two purposes. It must amplify the signal by a factor of two and shift it into the .5V-4.5V range (by adding DC) and it must eliminate higher frequencies. The frequency performance specification is given below in Figure 2. (Note that the response amplitude is with respect to the passband gain.) The representative response shown is just to illustrate one of many filter responses that would meet this specification.

9.2 Preliminary work:

Find the Transfer Function of a Butterworth Filter that would meet this specification. Keep the number of poles to a minimum so that circuit complexity will be minimized. (Recall that the Butterworth Filter has poles equally spaced around a unit circle of diameter ω_o in the s plane. Your choice of ω_o does not necessarily have to be 2 KHz.) Verify that your designed transfer function satisfies the specification using MATLAB. You would like to have a bit of margin for device tolerances and performance variations; you should not cut the corners too close. (You should make use of the handout on Butterworth filter design appended to the end of the syllabus.)

Design an active filter circuit using resistors, capacitors, and op-amps that will implement the transfer function. You will need to factor the function into cascade functions in order to make this easier. Use standard (available) values for components, especially the capacitors, and the 741 op-amp. (This may mean that you will not have exact values for the designed parameters; you should at least be close.) Model your circuit with PSpice, and run a frequency sweep to generate a Bode plot and see if it conforms to the specification given, and whether it is close to your predicted performance from MATLAB.

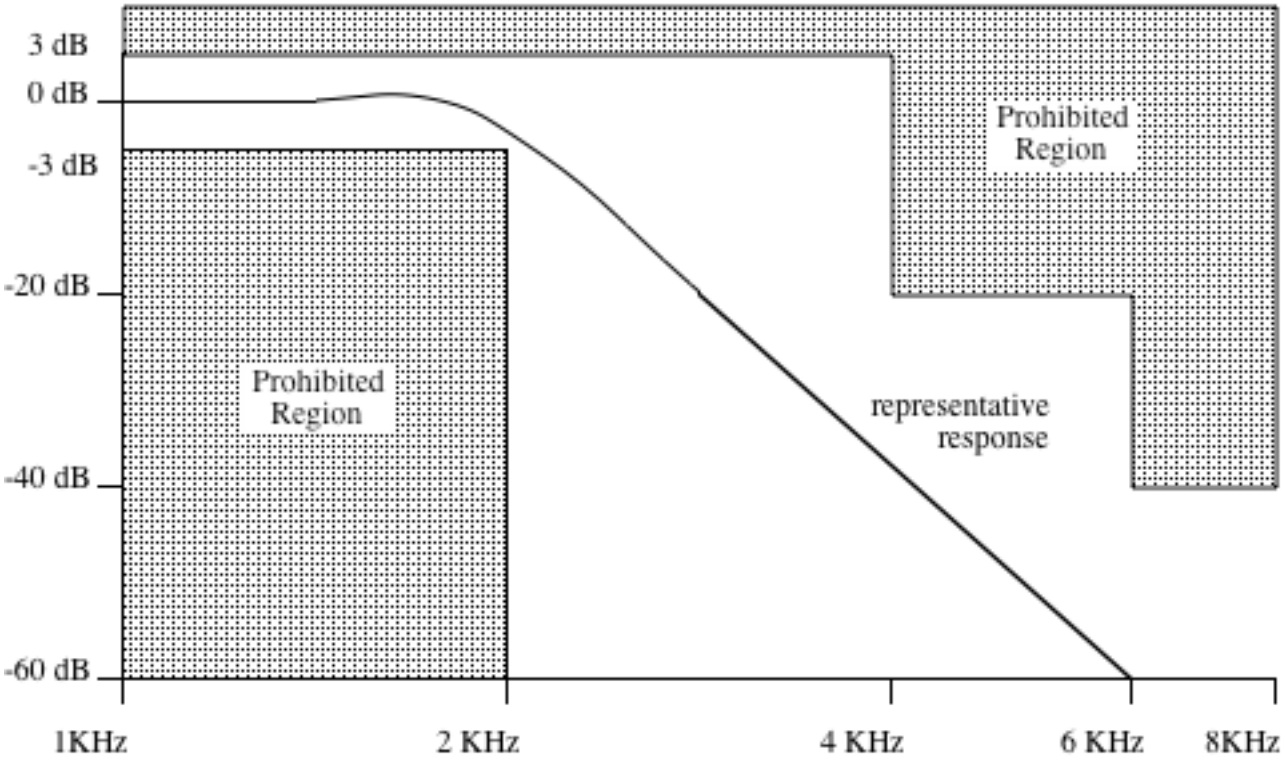


Figure 2 Low Pass Filter Response Specification

9.3 Laboratory work:

Build the filter. Perform a frequency sweep with a sinusoid signal ranging in frequency from 100Hz up to 100 KHz (maybe also with a narrower range) to assess the performance of your design. Note phase as well as amplitude for each sampled frequency. Be sure to include measurements for the key frequencies in the specification: 2KHz, 4 KHz, and 6 KHz.

9.4 Analysis and Report:

Write a formal laboratory report on what you have done, including an analysis of actual versus predicted performance, and reach a conclusion concerning whether your design should be utilized. Show your work, and justify your conclusions with your analysis. You do not need to include obvious details such as construction sequence; the schematics should speak for themselves. You should note anything unusual or interesting that you observe. You may want to include recommendations for further refinements, if that is necessary or would add value. (But, understand that in industry further refinements cost money and time; your manager wants a design that can be signed off and sent on to manufacturing as soon as possible.)

EE252 Electronics 2 Lab 10 Feedback and Stability

10.0 Objective:

To investigate the conditions for stability in loop amplifiers.

10.1 Pre-Lab Assignment:

In Figure 1 given that $R_1=R_2=R_3=10K$, $R_F=2K$, $R_S=1K$, $C_1=C_2=C_3=0.01\mu F$, and U1 is an LT1014 op amp (or, use four 741 op-amps), calculate the gain and phase shift, V_{OUT}/V_{IN} /φ. Draw a Bode plot from 100 Hz to 10 kHz. From your design equations and Bode plot, determine if this circuit will oscillate if V_{OUT} were connected to V_{IN}. If you decide that the circuit will oscillate, determine the frequency of oscillation. If you decide that the circuit will not oscillate, determine what has to change to make it oscillate. Simulate this circuit using LTspice or PSpice.

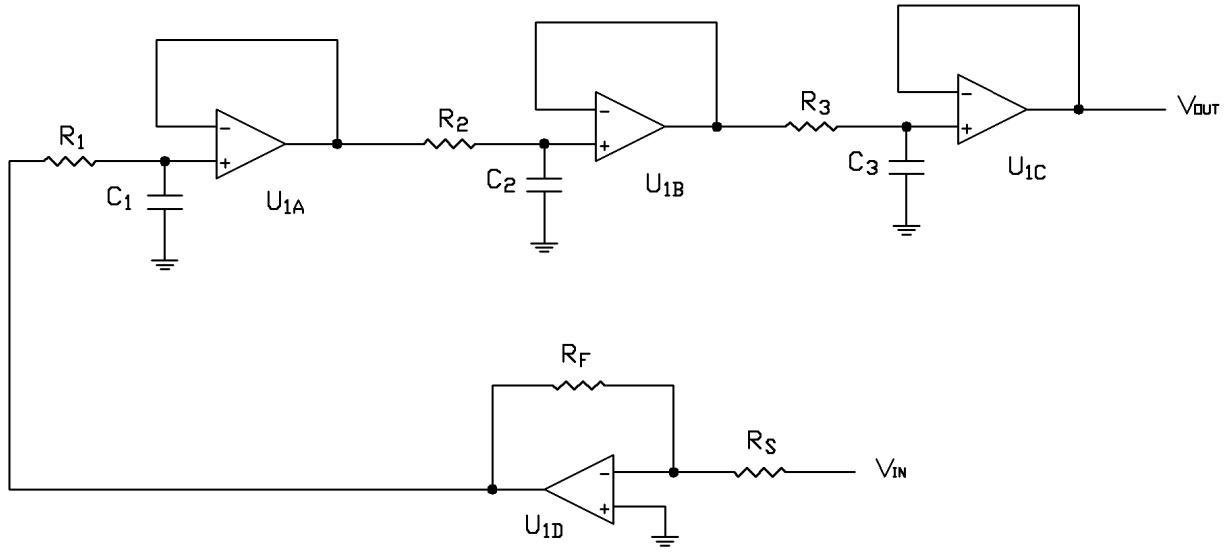


Figure 1 RC Oscillator

10.2 Lab Procedure: Build the circuit shown in Figure 1 and measure the open loop gain, V_{OUT}/V_{IN} and compare it to your design equations and the simulation. Do a frequency sweep to determine the phase margin and the gain margin (which will be negative if the circuit will oscillate).

Finally, connect V_{IN} to V_{OUT} and determine what ratio of R_F/R_S starts the oscillation. Describe the waveform at V_{OUT} and calculate the amplitude of the waveform.

Next, if the circuit oscillates, "compensate" the amplifier by inserting a pole in the first stage that will give a positive phase margin at the frequency of oscillation. Show that the circuit does not oscillate after doing this modification. Do a frequency sweep of the modified amplifier (open loop) to show that it should now have a positive phase and gain margin.

If the circuit does not oscillate (as first built), what needs to change for it to do so? Make the change, and do a Bode plot based on a frequency sweep to show that, as modified, the phase and gain margin are now negative. Then, demonstrate that it now indeed does oscillate.

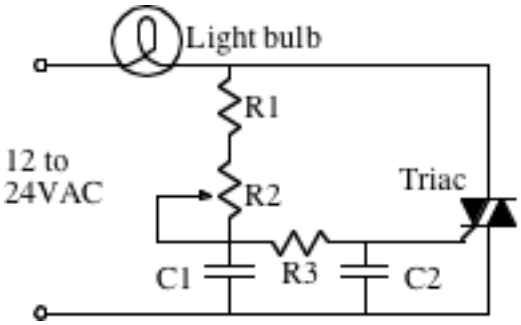
10.3 Report: Make a formal laboratory report. Include gain margin and phase margin of the open loop amplifier and the amplifier as modifies, answering the analytic issues raised.

EE252 Electronics 2 Lab #11: Triacs and SCR's
(This lab exercise may be modified.)

Objective: Develop an understanding of thyristors, particularly in control and switching applications.

Pre-Lab: Read this and come prepared. Get and look at a copy of the Triac data (Bournes TIC201M, Jameco (http://www.jameco.com) part number 1165690. Also, the SCR 2N5061 (Jameco part number 211422). (We might be able to use the MOC3011 Opto-isolator triac. Look up the data sheet for that, which includes some sample circuits.)

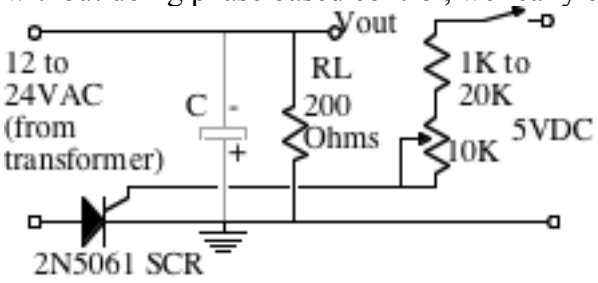
Check out the triac: Build the circuit below. Use adjustment of the potentiometer to vary the phase of the gate signal relative to the primary power to the load. Observe, and graph the AC waveform at the load for the extremes and middle position of the potentiometer.



Initially try R1=10K
R2 = 10K Pot
R3=10K
C1=.5uF (non-polarized!)
C2=.5uF (non-polarized!)
(at higher V, we would use a DIAC instead of R3, C2.)

L4. Modify your triac to trigger using the opto-triac and a current (limited by a resistor!) through the optical diode. Use the LED to turn a load on and off. (See MOS3011 data for the circuit.)

Check out SCR's: Build a half wave unfiltered power supply, but using an SCR instead of a diode. For simplicity, we build a negative Voltage supply. (This allows the gate Voltage to be referenced to ground.) Observe the output waveform under different gate currents (by varying the resistors in the gate circuit. (Normally a negative supply would include C. But if we do that, without doing phase based control, we really can only control on – off.)



Extra activity: Build a low or high pass filter for about 1KHz (using an Op-amp active filter perhaps). Rectify the op-amp output to produce a DC Voltage when the filter recognizes a signal. Connect the DC Voltage to a triac (AC) source (the opto-triac circuit from above is a good choice) to control a load. You have just built one channel of a color organ. Give your schematic, and a description. Try it on some music if you'd like. What amplitude in-band AC signal is needed to trigger the triac consistently?

Report: On a page, put the circuits you used with the waveforms observed to the load (light bulb) under different conditions for both the triac and SCR. Give answers to the questions asked in the lab exercise. Turn in the report at the end of the lab period.

About Input Impedance
September 2, 2006

Background:

We are often interested in designing amplifiers which have a high input impedance. The intent is that the amplifier does not present much of a load to the source providing the signal. The reasons for this may be varied, but we ultimately come to the issue of how to achieve this high input impedance while using bipolar transistors, which typically have a low base to emitter impedance. There are several ways to do this, each with advantages and disadvantages. Here we will look specifically at common emitter amplifier circuits.

Example problem:

Let us suppose that we are trying to achieve an input impedance of 10K Ohms, using a bipolar transistor with a nominal Beta (h_{fe}) of 100. We will drive a load that is a resistance of 1.5 K Ohms. Power supply Voltage is 10 Volts. We will assume the circuit is only to use resistors and capacitors in addition to the one transistor. There are three approaches we could consider. Each has advantages and disadvantages.

Approach 1: Choose IC so that the transistor's input impedance meets the specification.

This is perhaps the simplest approach. See Figure 1. The transistor presents an input impedance, or resistance if we ignore frequency issues, of r_π. This resistance depends on the Base current, and hence the Collector current. If we choose I_C = .22 mA, then I_B = .0022 mA, and r_π = 11.4 KΩ. Using a bias network current of about 10 times I_B, we can meet the input specification of 10K Ohms (10.3K actually). We fully bypass the emitter resistance, so that it has no effect on the AC gain.

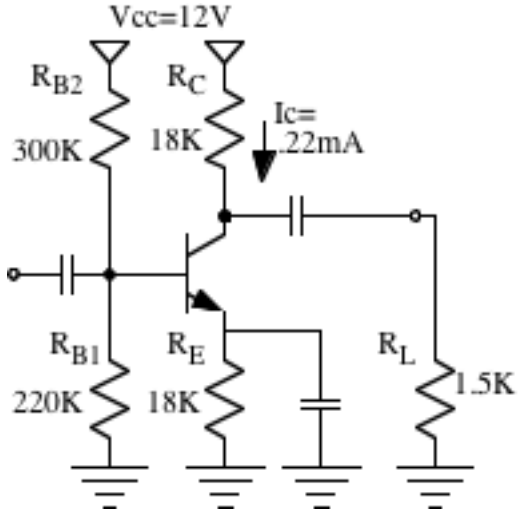


Figure 1: Common Emitter Amplifier with
High Input Impedance due to low Ic

The disadvantage of this amplifier is that it has a high output impedance (18K Ohms, that of the collector resistor, neglecting the transistor r_o). Thus, the voltage gain will vary greatly with the nature of the load. For the load of 1.5K Ohms shown, the Voltage gain is calculated with the formula below. (The gain factor is actually negative if we are interested in phase.)

$$A_v = \frac{v_{out}}{v_{in}} = \frac{i_c (R_C \| R_L)}{i_b r_\pi} = \frac{\beta (R_C \| R_L)}{r_\pi}$$

For the circuit values chosen, the Voltage gain comes out to be a factor of 12.2.

The disadvantage of this circuit, its high output impedance, could be a problem if stable gain is needed but the load varies. Also, if the transistor Beta varies, so will the input impedence. Interestingly, since r_π is (for our simple transistor model) proportional to Beta, as Beta increases the Voltage gain does not change. The benefit we get is in the form of increased input impedence. So, gain will vary greatly with the load, and input impedance will very greatly with the transistor Beta. Whether this is desirable or tolerable will depend on the nature of the application.

Approach 2: Choose an unbypassed R_E to give the desired input impedance, while maximizing I_C in order to get a low output impedance.

This approach is illustrated in Figure 2. Here, the value of R_C, which is critical to output impedance, is set to a relatively low value. Since it is the same as R_L, this gives relatively efficient transfer of power to the load. However, with I_C=2 mA, the value of the transistor's input impedance is only r_π = 1250 Ohms, far from the desired amplifier input impedance of 10K Ohms. Furthermore, to get base bias network currents about 10 times the base current, relatively small values must be used for the bias resistors, which also modify the input impedance downward. So R_{E1} must be chosen so that the transistor base appears to be a load of about 30K Ohms to the input. This is achieved with a 300 Ohm emitter resistor, since the impedance is given by:

$$R_{Bin} = r_\pi + R_E(\beta+1)$$

One can see the reason behind this formula thus: The base current coming in sees the r_π resistance and the emitter resistance. But for every unit of current coming in the base, the current in the emitter resistor has in addition a collector current component equal to Beta times the base current. So the voltage across the emitter resistor goes up Beta plus one times as much as it would in response to the base current alone. So, to the base, it looks like its resistance is Beta plus one times as large as it actually is. We get an overall amplifier input impedance of 10.1 K Ohms, meeting the specification.

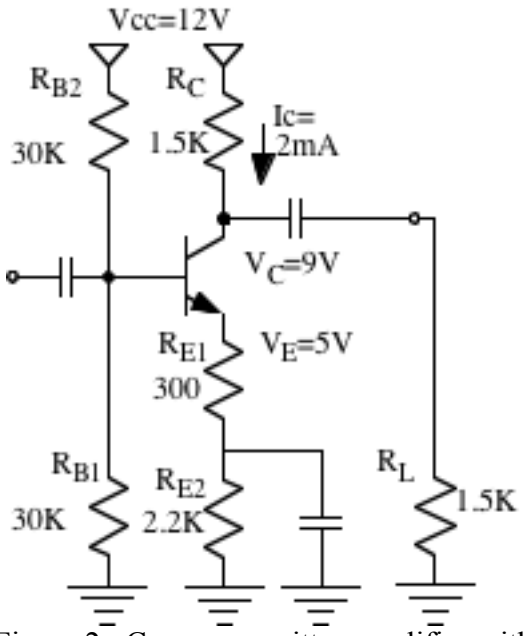


Figure 2: Common emitter amplifier with
Emitter feedback to give a high input impedance

The amplifier gain is now also affected by the emitter resistor, as given in the formula below.

$$A_v = \frac{v_{out}}{v_{in}} = \frac{i_c (R_C \| R_L)}{i_b (r_\pi + R_E(\beta+1))} = \frac{\beta (R_C \| R_L)}{r_\pi + R_E(\beta+1)} \approx \frac{(R_C \| R_L)}{R_E}$$

Notice that if Beta is high so that R_E times Beta is much more important than the effect of r_π, then Beta disappears from the equation! In this case, there's almost an order of magnitude difference, so the disappearance of Beta from the gain is only a rough approximation. For the numbers given, we get a gain of a factor of 2.8, less than one fourth of the value of the earlier approach.

Clearly this design, which meets the input impedance specification, has a major disadvantage compared to the previous design: the gain is much lower, by a factor of about 4. A significant factor of this loss of gain is the signal energy lost in the bias resistors, which must be compensated for by using a larger emitter resistor to give a transistor input impedance of 30K rather than something closer to 10K. If the bias was being provided through a choke or direct coupling to the previous stage, this difficulty would go away. Another disadvantage of this design is that, to get the bias resistors near optimality for input impedance purposes, the DC emitter voltage had to be pushed up to 5 Volts, unusually high, reducing dynamic range somewhat.

However, this design also has significant advantages over the previous one. The overall gain is somewhat less sensitive to the Beta of the transistor. Since the input impedance is more dependent on the bias resistances, the input impedance is also somewhat less sensitive to Beta. Most importantly, the output impedance is much lower (by more than an order of magnitude, 1.5K Ohms compared to 18K Ohms, so that the gain of this amplifier will be much less sensitive to variations in load. Are these advantages enough to outweigh the reduced gain? It will depend

on the nature of the application.

Approach 3: Additional resistance at the Base to increase input impedance:

This approach is simpler that that of number 2 above, but permits higher collector currents (and hence lower output impedance) than the first approach. A normal common emitter amplifier with no unbypassed emitter resistor is modified by the addition of an input resistor of a size needed to give the desired input impedance. Figure 3 illustrates. This is essentially the same design as the second circuit, but with the elimination of the unbypassed emitter resistor and the addition of the input resistor Ri. The input impedance is simply that of the input resistor plus the bias resistors and r_π all in parallel,, giving 10.25K Ohms in this case. (A lower DC emitter voltage would probably have been desirable rather than keeping the same operating point, but using the same bias network allows more direct comparison.)

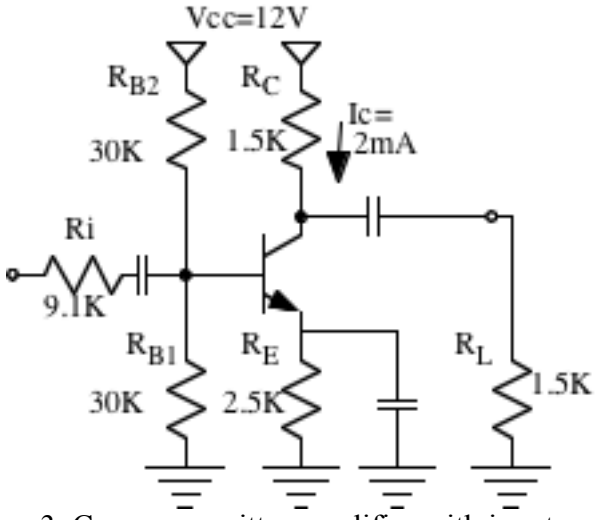


Figure 3 Common emitter amplifier with input resistor

The DC gain now is modified by the voltage divider formed at the input of the amplifier:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{(R_{B1} \| R_{B2} \| r_\pi)}{R_{in} + (R_{B1} \| R_{B2} \| r_\pi)} \frac{\beta (R_C \| R_L)}{r_\pi} \approx \frac{\beta (R_C \| R_L)}{R_{in}}$$

For the design above, we get a Voltage gain of 6.75. If R_{in} is much larger than r_π(in this case it is almost an order of magnitude greater) and the bias resistors are large, then the formula is approximately the ratio of input to output resistance times Beta. (That gives a factor of 8 gain, not very far off for this case.)

Compared to the other two designs, this one is intermediate in Voltage gain for the nominal conditions. It has one advantage over the others: the input impedance is less insensitive to variations in the transistor Beta, since it is mostly determined by the input resistance. In addition, this design has the same relatively low output impedance of the second design. However, this design, more than either of the others, has a gain that depends directly and proportionally on Beta. Transistor Beta is a notoriously unpredictable characteristic. If having a known (or stable) gain is desired, this is not a good design approach. On the other hand, if you happen to get a transistor with unusually good gain, you can take advantage of it. But beware:

too much gain can cause clipping and distortion in a later amplifier stage. So, like the others, this design has advantages and disadvantages.

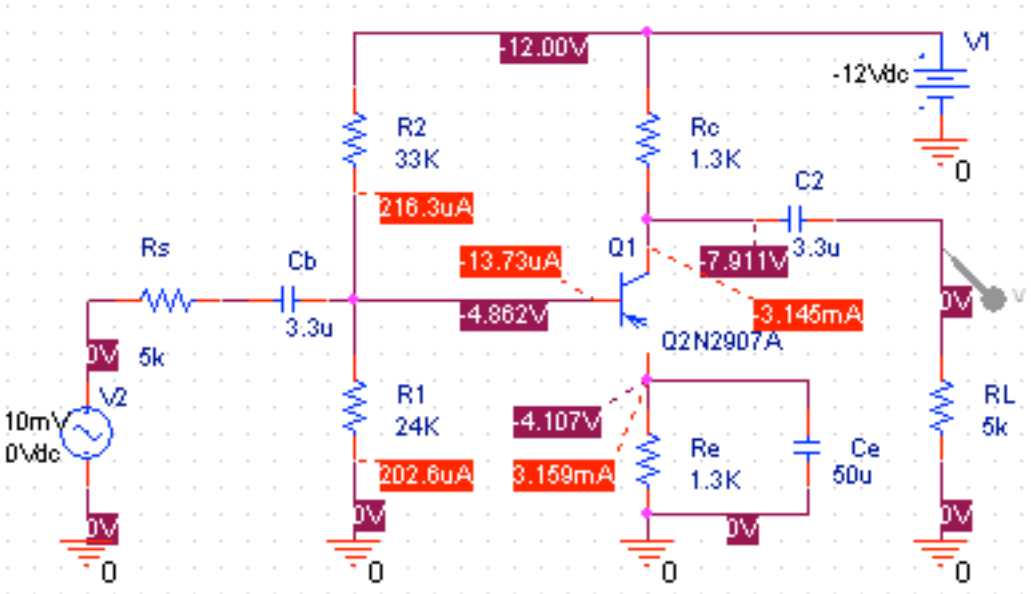
In practice, you simply do not see input impedance increased by just throwing in a resistor like this. Instead, the output impedance of the previous stage is increased to give the same effect, without adding a component, and with the benefit of helping the previous stage's gain.

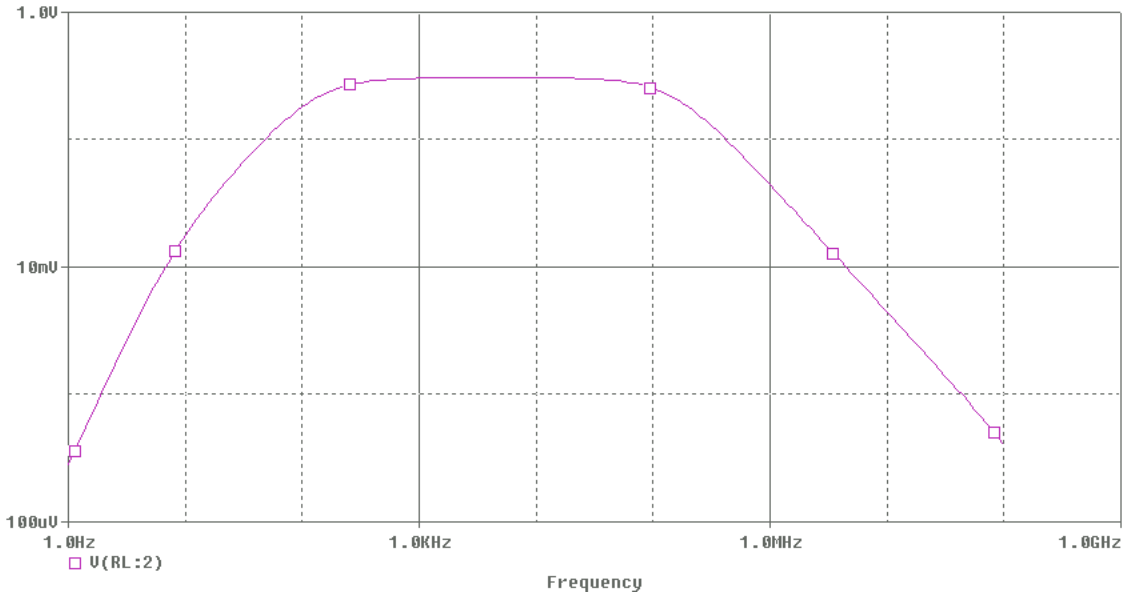
Summary:

In the design of a common emitter amplifier, there are lots of considerations and tradeoffs. These three design approaches each have their advantages and disadvantages. If stable well controlled performance insensitive to transistor characteristics is desired, design approach 2 is usually used. This is actually the most commonly seen approach, although in audio circuits where the overall gain is arbitrary, as determined by the user with a volume control, the first approach is also common. In higher frequency work where parasitic capacitances come into play, the disadvantages of design approach 3 are increased since the effect of collector to base capacitance is much worse than in approach 2. But that's beyond the scope of this document. The point is, this is not all a matter of following well defined procedures. There are many considerations, and ultimately the needs of the application will determine what approach should be used.

EE252 Simulation Amplifier Comparison

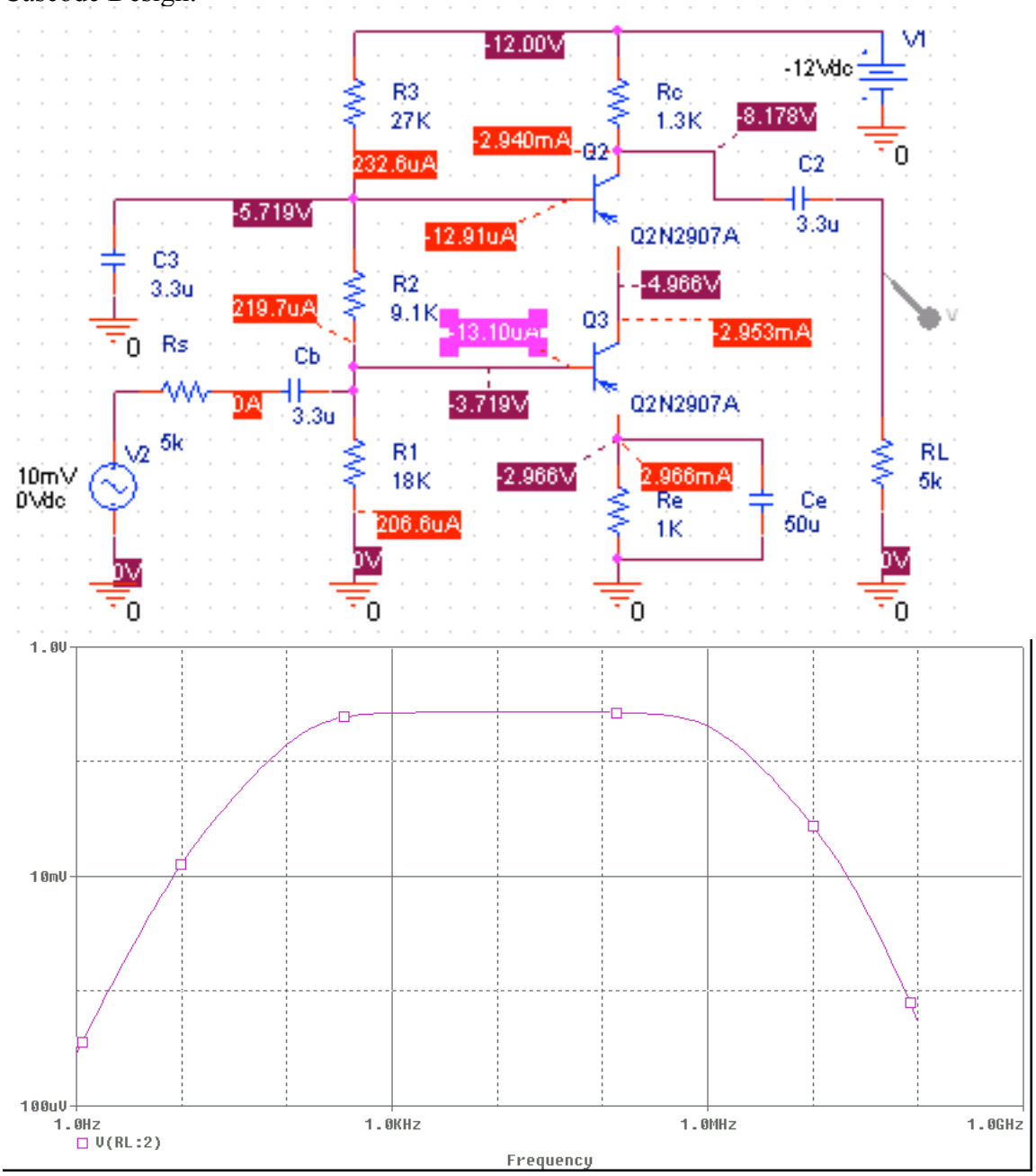
Common Emitter:





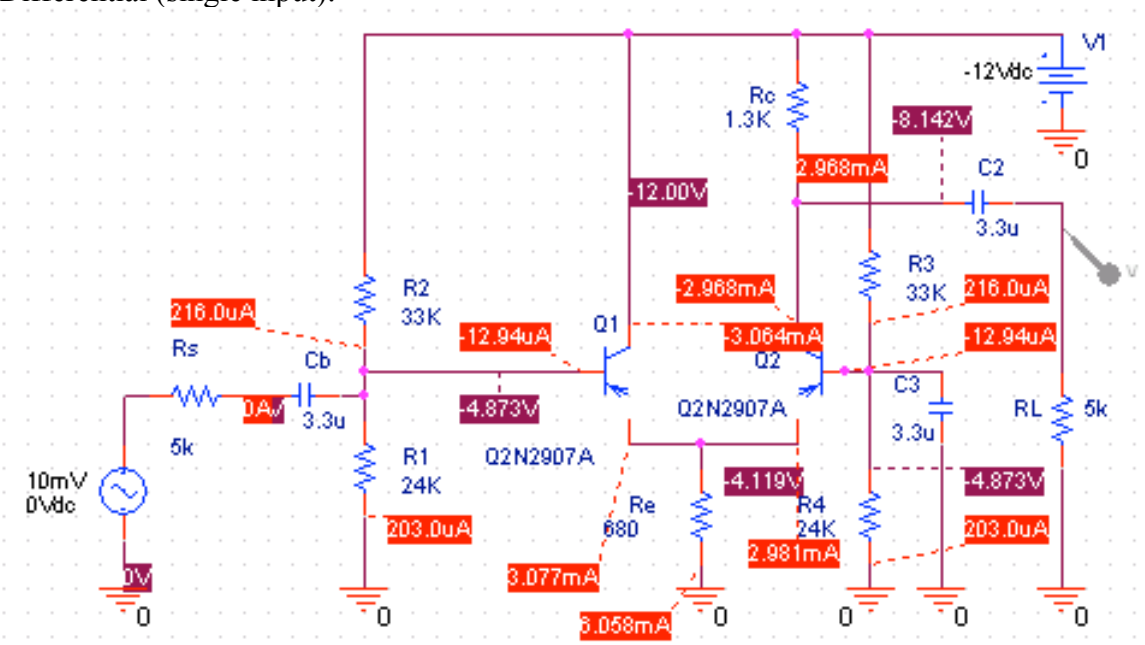
Output amplitude about .3V rms so gain from Vs = .3/.007 = 43 (33dB)
High frequency cutoff is at about 300KHz
Low frequency cutoff is at about 100 Hz as expected

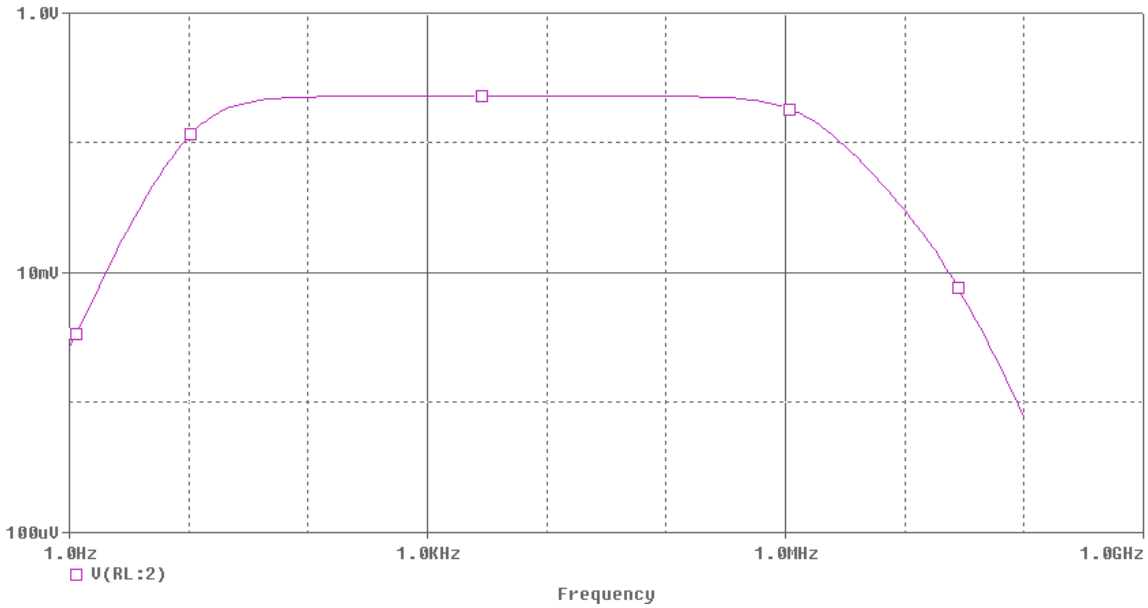
Cascode Design:



Output amplitude about .3V rms so gain from Vs = .3/.007 = 43 (33dB)
High frequency cutoff is at about 1.5 MHz
Low frequency cutoff is at about 100 Hz as expected
Better high frequency response than CE, and about the same gain, at the cost of more components and complexity. (The gain seems slightly less than for CE.)

Differential (single input):





Output amplitude about .2V rms so gain from Vs = .2/.007 = 29 (29dB)
High frequency cutoff is at about 2 MHz
Low frequency cutoff is at about 10 Hz (Output capacitor not reduced as intended)
Better high frequency response than CE, and but less gain, at the cost of even more components and complexity.

Butterworth Filter Design
for EE252 Electronics II
September 21 2006

A Butterworth filter is a design approach to positioning the poles of a high or low pass filter such that maximum flatness in the passband is achieved. To accomplish this, the poles are uniformly distributed around a circle in the S plane having a diameter equal to the cutoff frequency. The poles that would be on the positive half of the plane are ignored, so a 2 pole Butterworth filter has poles at + and - 45 degrees from the negative S axis, as shown in Figure 1 below:

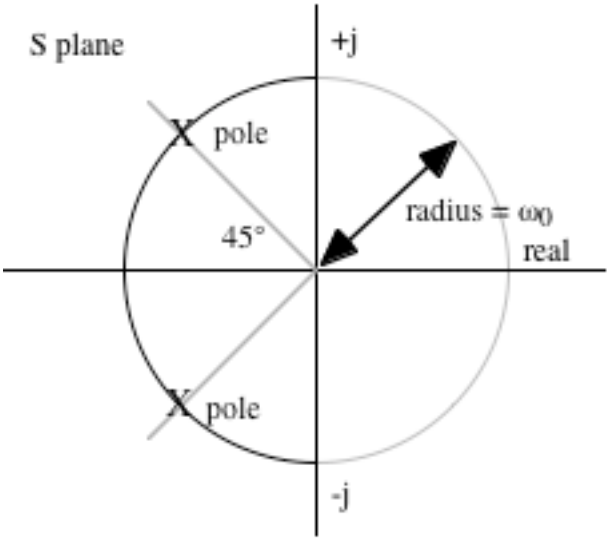


Figure 1: Pole positions for 2 pole Butterworth filter

The textbook, Microelectronic Circuit Design by Jaeger and Blalock, describes on pages 802 and 803 the process for implementing a two pole Butterworth filter using an op-amp. The issue addressed here is how to do so for a higher order Butterworth filter having more than two poles. There are various ways this could be done, but for simplicity we will assume here that the filter will be constructed of a cascade of sections, each of which is itself a first or second order filter. Overall, we still need to put the poles on the unit circle, but now there are more poles. A three pole Butterworth would have a complex conjugate pole pair at 60 degrees above and beloiwe the axis, and one real pole at minus ω_0. These would be built with a first order filter followed by a second order filter (for the conjugate pair).

When building higher order Butterworth filters, note that the second order sections are not the same. Each must implement a complex conjugate pair for a different spot on the unit circle. This is illustrated below by a design example of a four pole low pass Butterworth filter. The pole positions must be as shown in Figure 2. We will assume that the cutoff frequency is 2 KHz.

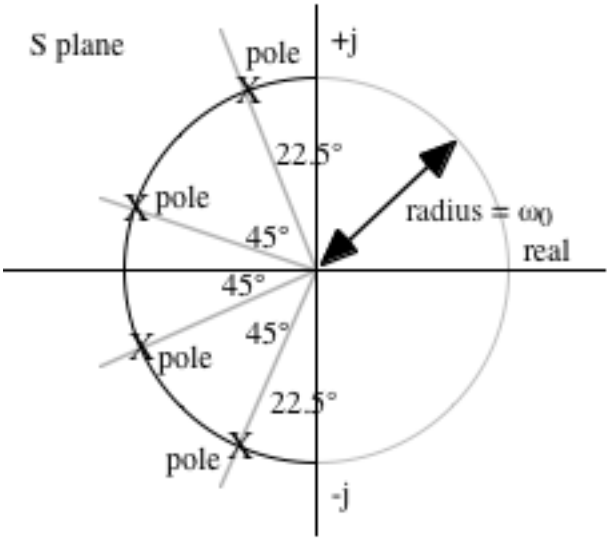


Figure 2: Pole positions for four pole Butterworth filter

The next task is to determine what the actual pole values are, and then from that derive the corresponding Q for each filter section. Each pole pair has a value of -a ± bj, where a = (cos θ) ω_0 and b = (sin θ) ω_0. ω_0 = (2 KHz) (2π radians / cycle). So:

First pole pair at θ = ± 22.5 ° : a = 11.61 K rad/sec b = 4.81 K rad / sec
Second pole pair at θ = ± 67.5 ° : a = 4.81 K rad/sec b = 11.61 K rad / sec

Each filter section (assuming unity gain) has a transfer function of:

$H(s) = s^2 / (s^2 + (\omega_0/Q) s + \omega_0^2)$.

We know $s^2 + (\omega_0/Q) s + \omega_0^2 = (s + a + bj) (s + a - bj)$. We know a and b for each pole, as well as ω_0. So for the first pair, we can calculate that Q = .54, and for the second pair Q = 1.31. Now it is a matter of finding C1, C2, R1, and R2 for each section.

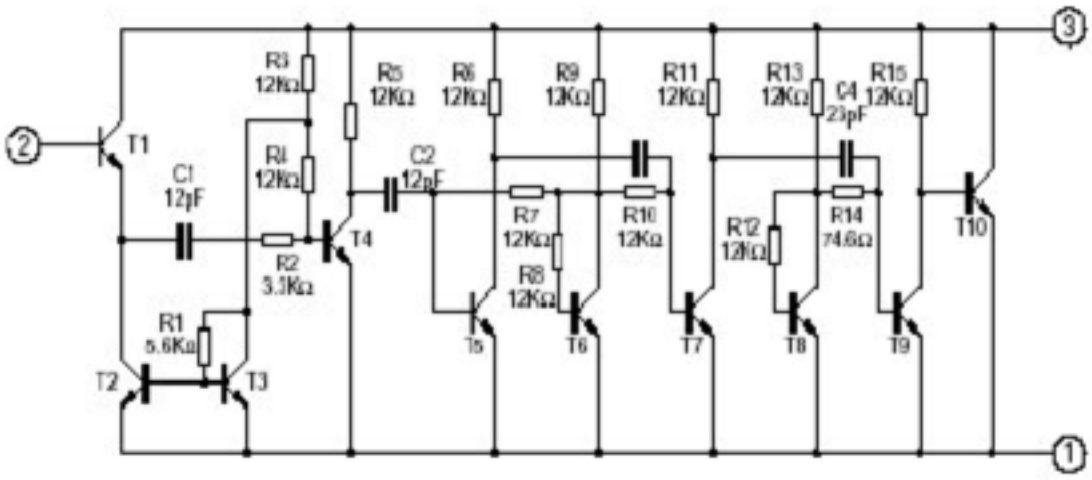
For the first section, having Q = .54, we have two known values, Q and ω_0, and four component values to determine. We have two equations to use:

$\omega_0 = 1 / \text{sqrt}(C1\ C2\ R1\ R2)$

$Q = \text{sqrt}(C1 / C2)\ \text{sqrt} (R1\ R2) / (R1 + R2)$

This is an underconstrained problem. However, we can play around with it and soon find that if C1 = C2, we can never get Q > .5. So we ultimately will need different C values. Suppose we start out assuming R1 = R2. What value should we pick? Since we do not want to use the larger, more expensive capacitors, we will use larger resistor values, say, 10K Ohms. Given that, C1 C2 = .0213 μF^2 to get the ω_0 we want.

MK 484 RF amplifier IC Internals



Things of interest:

This device has only three terminals! The power pin (3) also serves as the output. This is possible because the device operates at high (RF) frequency, but the output is at a low (Audio) frequency, so an external capacitor that bypasses the power supply for RF purposes passes the signal for audio. The last transistor's collector is the output; this stage is actually common emitter even though it looks a bit like common collector.

Notice the current source that serves as the emitter resistor for the initial common collector input stage. This is what gives the input such a high impedance, which is very helpful in achieving a high "Q" for the resonant tuning circuit.

This is an IC, and it does include four capacitors. But notice that the capacitance values are very small; the biggest is just 23 pF. That's big enough for coupling purposes apparently because the frequency is up in the MHz range.

Notice that all of the transistors are NPN. That reduces the number of manufacturing steps, and hence the cost. All of the emitters are actually at the device ground, which should allow vertical transistors, with better performance, with T1 being the one exception. Most of the resistors have the same value. Using a TO-92 3 pin package also reduces cost. The device runs on a 1 1/2 Volt battery, which reduces the costs to the user of the device. Economics has an important role in practical electronics.

The feedback circuit (around T6) is interesting. This gives negative feedback to the corresponding common emitter amplifier T5. Without this, there are enough phase shifts and coupling back through the power supply that the amplifier would oscillate. T6 and T8 seem to be involved in properly biasing T5, T7 and T9. Understanding these circuits would take a good bit of analysis.