EE-345, Computer Organization

Fall, 2017

Text

David A Patterson and John L. Hennessy,
Computer Organization & Design The Hardware / Software Interface
4th ed., Morgan Kaufmann

Class Times & Location

MWF, 9:00-9:50AM
SLC216

Instructors

Mike Morrow
John B Gilmer Jr.

Office Hours & Location

TBD and *TBD*. Phone: *TBD*. Email: *TBD*.

Overview of the Course

At completion of the course, the successful student will:

- Show familiarity with CPU architectural (ISA) features
- Have an understanding of the construction of in-order scalar CPU's
- Know, in general, how a memory hierarchy operates
- Display familiarity with SystemVerilog RTL simulation and synthesis

Web collateral

URL is *TBD*.

All lecture notes, assignments, examples, etc., will be available on the web. I'll endeavor to get them up within 24 hours after each class.

Grading

All items will be graded on a scale of 0…100, with weight as shown below.

Item	Weight	Notes
Two tests	25% each	
Final	35%	
Assignments	15%	Approximately weekly

At end-of-term, the totals will be combined and scaled into the Wilkes 4.0 grading system:

Total	Grade	Total	Grade	Total	Grade	Total	Grade
> 92	4.0	87-83	3.0	76-70	2.0	64-60	1.0
92-88	3.5	82-77	2.5	69-65	1.5	< 60	0.0

Assignments

Most of the assignments will be projects where you create/modify code. I say "code" because even though this is a hardware class, we'll be expressing things in Verilog and assembly language. In some cases, we'll load the code into an FPGA.

I anticipate you'll work on projects in groups of 2-3 students, although an occasional assignment will be mandated as "solitary". You may hand in a single object to cover all of the people in a group, just be sure that all the contributors' names are listed, so you each get credit!

Topics and Schedule

Below is the approximate schedule. We may linger on some topics, and blaze through others, so I can't guarantee we'll absolutely stick to this!
Note that the text tends to be light on hardware details, so I've added an "extra topics" column – these are items we should discuss that aren't well represented in the book. You'll be reliant on the lectures for this material, as well as any good web references we can identify.

date	week	class hours	topics from text	extra topics	text
8/28/2017	1	3	overview, basic system arch, basic CPU architecture, measuring perf	Intro Verilog, intro RTL sim	Ch 1
9/4/2017	2	2	number representation, instr encoding	Intro Verilog	Ch 2
9/11/2017	3	3	Instruction Set Architecture details	Tools: ISS, assemblers	Ch 2
9/18/2017	4	3	Assembly language		Ch 3
9/25/2017	5	3	Comparative architectures, architecture vs. uArchitecture, CISC, RISC	Intro to timing	Ch 2
10/2/2017	6	3	Datapath	More Verilog, synthesis, uProgramming, SAP2	Ch 4
10/9/2017	7	2	Intro to pipelined machines	**Test #1** EZMIPS architecture	Ch 4
10/16/2017	8	3	More on pipelined machines: hazards (data, control, structural), bypass/forward logic	Coding guidelines	Ch 4
10/23/2017	9	3	More on pipelined machines: arbitration, holds, dig into each stage		Ch 4
10/30/2017	10	3	Exceptions (and interrupts)	Speculation	4.9
11/6/2017	11	3	Caches (I, D, unified)	**Test #2** Design flow (ASIC and FPGA)	Ch 5
11/13/2017	12	3	Virtual Memory	Floor planning, incl. clock, pwr	Ch 5
11/20/2017	13	1		Caches combined with virtual memory	
11/27/2017	14	3	Parallelism		Ch 7
12/4/2017	15	3	System architecture		Ch 6
12/11/2017	16	1	exam	**Exam**	