Appendix G
Example Laboratory Exercise where Things Go Wrong

Introduction:

This appendix follows a "Lab 4" laboratory exercise in EE252 that was designed to provide surprises. The intent here is to give an example of how to deal with issues when surprises, seemingly wrong behavior, occur in the laboratory. The origin of this appendix is an email message that was sent to the class after the laboratory reports were received several years ago. That response has been modified here to include enough of the lab exercise instructions and results to provide a context for understanding the context.

Background (to the students):

There seemed to be some misunderstanding about what the laboratory exercises are about. Yes, they are design exercises. The context is sort of like what you can expect in industry: you are expected to design something and then build a prototype and see if it meets expectation. The report should compare what the circuit or system did compared to what it was specified or designed to do. But these lab exercises are intended to also be a learning opportunity – an opportunity for discovery. This was particularly true of this lab exercise. There were several surprises to be discovered, and learned from, along the way. I'd like to review those.

You should have come into the lab exercise with a basic understanding of the three types of bipolar amplifiers: common emitter, common collector, and common base. Common base is the least frequently encountered, but still has its important uses. Briefly:

Common Emitter: Good Voltage gain of $A_V = -g_m (R_C \,||\, R_L)$. Current gain is also good. Decent $R_{in} \sim r_\pi$. Decent $R_{out} \sim R_C$. It has that 180 degree phase shift that creates the Miller effect, limiting high frequency performance.

Common Collector: Only a bit less than unity Voltage gain, but high current gain of about $\beta(R_E/(R_E+R_L)$. Good (high) $R_{in} \sim r_\pi + (\beta+1)(R_E||R_L)$. Good (that is, low) output impedance of $R_{out} \sim (r_\pi + R_S)/(\beta+1)$. Everything is good except no Voltage gain!

Common Base: Good Voltage gain of $+g_m(R_C||R_L)$ – the same as common emitter. Less than unity current gain $A_i \sim R_C/(R_C+R_L)$. How can that be? Because anything you gain with A_V comes at the expense of a very, very low input impedance of about $r_\pi / (\beta+1)$. $R_{out} \sim R_C$, the same as common emitter. But, there's no Miller effect since there is no phase inversion.

You have seen what a common emitter amplifier can do. Now you take the same parts and reconfigure them as Common Base. Instead of grounding C_E, you use it as an input. Instead of using C_B as the input, you ground it. It's as simple as that. So, coming up with the circuit itself is easy. The Q point and components are the same. But a design is more than just a circuit. The design process should also indicate what's

expected of the circuit. Most important is gain. You calculate $A_V = g_m (R_C||R_L)$ or some equivalent formula to get just as much gain as you got from the common emitter circuit. That is, if you define A_V as v_{out} / v_{in} where v_{in} is taken at the input of the amplifier.

The Laboratory Exercise:

The laboratory exercise had two phases. First the student was to design and build a common base amplifier and find its "midband" gain and input impedance. A common collector output stage would then be added. The initial amplifier is shown in Figure L-1 and the amplifier with the common base stage in Figure L-2.

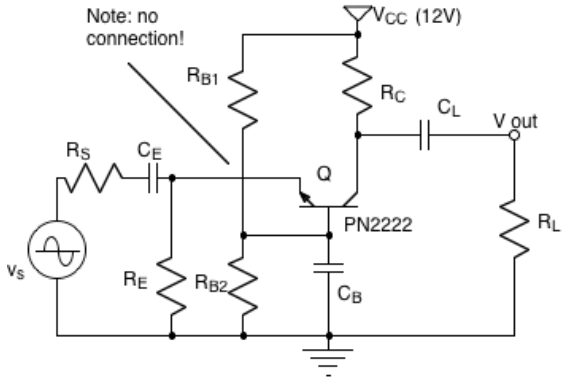

Figure L-1 Common Base Amplifier

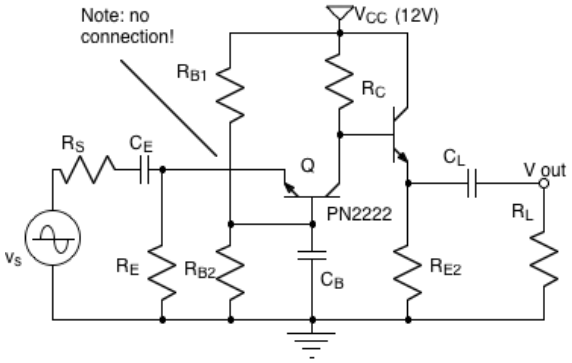

Figure L-2 CB amplifier with CC output

A typical design operating point has Collector Current I_C=1.0 mA, V_{CC}=12V, V_C=8V, and V_E=4V. Using nearest standard values, R_C = 3.9KΩ, R_E=3.9KΩ, R_{B2}= 47KΩ, R_{B1}=68KΩ should give that operating point, a problem students solved in a previous exercise. R_L is specified as 1.0KΩ, and R_S as 100Ω. Capacitor values of C_E = 470μF, and C_B, and C_C both 10μF, should give a midband good for 1KHz. Using the gain formula, a student would expect the Voltage gain:

A_V=gm ($R_C||R_L$) = 38.5 mS (3.9KΩ || 1KΩ) = 38.5 mS (.796KΩ) = 30.6 (V/V)

If the student simulates the circuit with R_S of 100Ω, and when built in the lab, the gain is much smaller! This was (typically) a surprise. Something has gone wrong! This is the first of several surprises in this exercise.

Discovery #1:

Here's an opportunity for a discovery. In the lab (or in simulation) you add in the R_S=100Ω, and measuring A_V you come up with maybe 10 (6 or 7 for the example case). You had calculated something on the order of 100 (in the case above, 30). At this point, several things ought to happen:

1) First, you need to notice that there is a discrepancy. This means recognizing that your role in this lab exercise is more than just following directions, taking data, and compiling it. You need to be thinking about what is happening, and whether it is what you should have expected. If you see a factor of 10 difference between designed gain and actual gain, or between simulated gain and actual gain, you need to notice. It helps

if you have a table in your results section where you list things like Q point values and gain side by side for design expectations, simulation, and lab results.

2) Second, you need to care. It is possible to take the attitude of, "Yeah, there's a big difference, but why should I care? I'm just doing what the lab directions say to do. Once I throw this lab report into the hopper, what difference does it make?" This is not the attitude you want to take to the job market. You should try to be developing an inquiring mind now. These laboratory exercises are designed to present you with surprises like this one. Take the opportunity. Be curious. Wonder what is happening, and why. Is there something from theory that could explain the phenomenon?

3) Third, you need to try to explain things. Why should this happen? A factor of 10 difference in gain can't usually be explained by variations in the values of 5% tolerance resistors. Don't just guess. You are becoming an engineer, not just a hacker. Don't just look for excuses, as if it's your fault that you built something wrong and want to avoid the blame. In this case, such a discrepancy is actually expected. It's part of the learning exercise! You have a base of theory which should help you understand things. Try to apply it. How to do that?

4) Using your knowledge of theory, construct hypotheses about what might have gone wrong. Then test those hypotheses by making measurements of the operating circuit. The first hypothesis ought to usually be, "Is my transistor operating in the linear range?" That is usually equivalent to, "Is the Q point right?" If you forgot to turn on the power supply, it won't be. Easy to find and fix. But a gain discrepancy is something else. Is the transistor in backwards? Many transistors will amplify with C and E reversed, though with a lousy β. Ultimately, you should follow the signal through the amplifier and see what happens to it. (In more complicated systems it is also useful to inject a signal part way through and see what comes out.)

In this case, when you start probing the circuit, you should note the difference in Signal (AC) Voltage on either side of the RS=100Ω source resistor. There's a big difference! The signal almost disappears at the input of the amplifier. Why? Going back to theory, the R_{in} of the amplifier is very low. In effect your source is driving a Voltage divider, and the amplifier is only getting the leftover under the 100Ω resistor. So at this point, you should be asking yourself, "Exactly how did I define A_V?" Is it v_{out}/v_{in}, or v_{out}/v_s, where v_{in} is the AC voltage at the input of the amplifier (after the resistor) and v_s is the AC Voltage from the Thevenin equivalent source before the resistor? If you have a big discrepancy, then you probably calculated A_V one way but measured it another way. Perhaps you were a student that figured this all out. If so, good for you! But the greater learning occurs when you found a discrepancy, then went back and found the error in your design work, and corrected it by making the method for calculating A_V consistent for all three methods: design, simulation, and laboratory.

Discovery #2:

So, we are faced with the fact that from our original signal source, the gain is lousy even though from the input of the amplifier it is decent, just as good as common emitter. Even if you get rid of the 100Ω R_S, the signal at the amplifier input is much less

than that you dialed up on the signal generator, because of the 75 or 50 Ω output impedance that it has. You can't reach inside the signal generator to get to that perfect zero impedance source. It doesn't exist. And, it doesn't exist in most other signal sources.

All of this demonstrates that the very low R_{in} of the common base amplifier costs us something. It costs us gain anytime the source impedance is not also very low. So, you need to think of that when you are choosing what kind of amplifier to use. For example, a crystal (piezoelectric) microphone has a very high output impedance. You don't want to use a common base as the first stage of your audio amplifier. On the other hand, a magnetic microphone (or PM speaker used as a microphone) has a low impedance. You could get by with common base for that if you needed to, say, to avoid the 180 degree phase shift.

For many practical cases, we need to find not A_V from v_{in}, but A_V from v_s, the Thevenin equivalent source. That means adding to the gain equation a term for input (or insertion) loss: $R_{in} / (R_{in} + R_S)$. When we add this term, we can accurately see the impact of using a common base stage with its very low input impedance. There are still times when we need to do this, since common base is the only way to get Voltage gain without getting the 180 degree phase shift. (OK, you could instead use a transformer to get V gain at the expense of I gain, but they are expensive, bulky, and heavy.) The same concepts also apply to FET's and vacuum tubes.

Adding the Common Collector Stage:

The lab exercise directions specified that R_{E2} and R_L would be 100Ω each. And Q2 would be another PN2222 transistor. The student ought to have calculated the Q point values for this variation of the circuit, and the consequent gain, which is the product of the gains of the two stages. Recall that the gain of a common collector stage is usually just a bit less than unity.

Discovery #3:

What happened when you added the Common Collector stage? What did you expect to happen? What actually does happen? There are actually two parts to this.

Discovery #3a:

You measure the Q point. You had V_C = 8V (or close to that) for just the Common Base amplifier. Now what do you have? Isn't it a bit less? Why should that be? OK, let me go through the steps again, quickly this time:

1) You need to notice.
2) You need to care.
3) You need to ask yourself why.
4) You should construct a hypothesis and test it.

In this case, step 4 isn't hard. If V_C is lower, there is more current going through R_C than before. But the bias circuit on Q1 has not changed; V_C should be the same. (You can check it. If V_C is still well above V_E, then I_C and I_E should be very nearly the same.

Checking V_E confirms that I_C has not changed significantly.) If the current is going through R_C but not into the collector, where could it be going? With just the Common Base transistor, a capacitor should have blocked any DC current from flowing through R_L. (If that capacitor was backwards, and leaking, you should have noticed the discrepancy between I_C and V_C.) There's only one place the extra current can be going: into the base of Q2. Is that large enough to make up for the observed difference? Well, apply theory to see. I_E for Q2 is easily calculated, and should come out around 60mA. If that is divided by β, that would be equal to I_B, the "extra" current through R_C.

Here, you may make a discovery: "β seems lower than it ought to be! I've been assuming 200, and the ratio of I_B to I_C for Q2 comes out less than 100!" So, again, you need to notice, care, ask yourself why, and come up with a hypothesis. Is the capacitor to the load backwards? That would increase I_E by the leakage through the capacitor and R_L. Or, maybe the β properties of a transistor vary. In fact, this is the case. We often assume for design purposes that β is a constant. It isn't; it's only approximately constant, and that's if we are considering a fairly narrow range of Q point currents, say in the .1 to 10 mA range. At 60 mA, the β is lower. Think about the TIP-31. At 1A the spec for β is "at least 25." At 3A it's only "At least 10." If you put a TIP-31 in your DMM and test it for h_{fe} (β), you might see 400. (Look back to EE251 material on BJT's.)

So, now that you have made this discovery, what do you do about it? What you ought to do is go back and correct your design calculations, specifically Q point, to reflect a somewhat different reality than you expected. This has potential implications for AC performance if β for Q2 is lower than expected. Check you AC gains, too. You want your design understanding to match reality as best you can.

Discovery #3b:

You measure amplifier gain, and you find that it's greater than with the Common Base (CB) stage alone. Did you expect this? Let's think about it. If you calculated gain for the CB stage, and if you use that same gain for the CB + CE design, then you expect gain to go down slightly, not up, when you add the CC stage, which has less than unity gain. Right?

At this point, you need to 1) notice, 2) care, and 3) ask yourself why. Something you assumed in your design calculations is not right. Time to start building debugging hypotheses. Let's suppose:

Hypothesis #1: Theory notwithstanding, the CC stage DOES give Voltage gain after all. This can be tested. Look at the AC signal before the CC stage (at the Q1 collector). That's even bigger than the output! So the CC stage has less than unity gain as expected, and the CB amplifies more than it did before. This is useful information, and should move us to:

Hypothesis #2: Something is wrong with "$A_V = g_m (R_C \,||\, R_L)$." Well, yes! The original R_L isn't in the circuit anymore! What has taken its place? R_{in} of Q2. So, calculate what that is and put it back into your gain equation. More gain! Aha!

So, finally, you should go back to your design work and fix this. You ultimately want your use of theory to explain what happened.

Discovery #4:

There's anoher possible reason for having less than the expected gain, even after taking into account the low input impedance effects. Are you in midband? Our gain calculations are for midband. We ought to see all the signals pretty close to exactly in phase. But if some capacitor is too small, then the signal will shift away from 0 degrees. This requires that you notice the phase. Did you? If you are not seeing 0 degrees, something is wrong, and that something has to do with AC. If you are at a low frequency, say 100 to 1K Hz, that's most likely a low end problem with one of the capacitors you put into the circuit, not a parasitic capacitance issue. So, you need to ask yourself, for each capacitor, "Is it big enough?" A hacker solves this by making all of them huge. Say, throwing 1F at each. But having a capacitor too big is a problem too. It's expensive, heavier, and bigger. So for practical cost purposes you want "just big enough." But electrically, a too-big capacitor makes your startup / power-on transients longer – it may take too long to reach the desired operating Q point. Even seconds or tens of seconds. Things are not stable on the scope. It's hard to understand what is going on; it seems random.

The engineering approach is to calculate where your poles are. What resistance does each capacitor see looking at the rest of the circuit? What is the corresponding time constant and frequency? Are all of those well below my operating frequency?

You were instructed to use a "big" capacitor for C_E. 10 uF is good for the capacitors on the base and collector. But is it adequate for the CC output coupling? Now we are driving R_L=100Ω. What is the output R_{out} of the CC stage? Looking into the emitter of the CC transistor, we see $(r_\pi + R_C)/(\beta + 1)$. This is very much like looking into the emitter input of a common base circuit. So, essentially, we see R_C divided by 100 or so, something less than 100Ω. So if R_C is about 100Ω times 10 uF, we only have a time constant of 1 msec, corresponding to a frequency of 160Hz. That's probably below the frequency you were using, or might be close enough to have an effect. Did you notice the phase shift? Maybe there wasn't one. But if there was, did you care? Ask why? If you did, you had an interesting discovery to make. If you were in too much of a hurry and failed the above wisdom and intelligence checks, you missed a learning opportunity.

Discovery #5:

So, if we connect CB+CC, we get some good gain and can drive a decent load. If we want to avoid the 180 degree phase shift of CE and its Miller effect, what other choice do we have? Well, we could have done CC then CB: same thing but cascaded in the other order. Well, that's nothing but a differential amplifier, with the signal applied to the "+" input and the output taken to ground instead of across the collectors. So, does differential do better? The short answer is "yes, at least sometimes". The input impedance is double what you get with CE (good!). The gain is half what you get with

CE (and CB alone). How can that be? Because the input impedance of the CB stage is so low, the CC stage gain is only ½ instead of being almost unity. The optional extra part for this exercise with the differential amplifier was supposed to help understand this. Unfortunately, that's just too much for this one lab exercise. Some of you will do a "Differential amplifier" later. Think about it as CC+CB when operated single ended.

Discovery #6:

Things in reality don't always match theory and simulation. Those wires back to the power supply are inductors. There's distributed capacitance everywhere. Electrolytic capacitors look like inductors, not capacitors, at high frequencies. Some of you saw the consequences in the form of 50 MHz or so oscillations. Those need to be suppressed. We used bypass capacitors for the power and added (or enhanced) high frequency poles in the circuit by putting small capacitors to ground at circuit nodes (the input node in particular). To understand oscillation, you need more theory than you have now. It's possible to get oscillation at low frequencies as well as high frequencies in multi-stage amplifiers. You will see other discrepancies between simulation and reality as we move into power amplifiers and especially the radio circuits.

Discovery #7:

So, your amplifier is operating in CB+CC mode and cooking away, pumping out a reasonably good gain consistent with your adjusted predictions. Hmmm, what's that you smell? You try touching components to see if they are hot. Ow! R_{E2} is indeed hot, maybe even smoking! Or, perhaps Q2 (the CC transistor) suddenly fails. How did that happen? Maybe you just assumed the transistor is bad, or just didn't even notice the hot R_{E2}. But if you did, you had a discovery to make. Why are these things hot, and possibly failing? What's a reasonable hypothesis? "Maybe they are dissipating too much power." That's usually what makes things hot. The question then becomes whether that is by error or fault in the components or circuit, or by the nature of the design. If you found V_{C1} to be about 7.5 Volts, then V_{E2} is .7V below that, around 6.8V. All the DC current through Q2 has to go through the 100Ω R_{E2}, so that resistor must be dissipating about .46 Watts. If it is a 1/4W resistor, it will get very hot and may fail. If it is a 1/2W resistor it will still get hot, but shouldn't fail. The transistor is also about at its maximum dissipation limit. It may fail. The resistor problem can be fixed: use a 1/2W resistor (or perhaps use two ¼ W resistors in series or parallel). For the transistor, it's a tougher problem. The best solution would be to use the 2N2222 transistor in the TO-18 package, electrically identical but able to handle more power (1/2 W). It's also possible to improvise a small heat sink for such transistors. Or you could use a different transistor that can handle more power. But that's beyond the scope of what we were prepared to do in the lab.

Conclusion:

Please, for the sake of your education, approach the laboratory exercises as an opportunity for discovery. Look for discrepancies. Ask why when you find one. Think about how theory might help explain what you see. Remark in your report on discoveries and how you explain them, or honestly leave the question open if you can't. The point of the lab report is not to prove that everything went right even if it didn't. You are (probably) not being graded with an emphasis on "Did you get the right

answer." Yes, there is a small penalty for mistakes, but the major reason for lost credit is leaving stuff out or ignoring things that don't come out right and treating them as if they did. I'd much rather see that you found a problem, and thought about it, even if you don't have an answer.