**EE283 Laboratory Exercise #2**
**DC Circuit Analysis**

**Objectives**:

1. To verify Kirchhoff's Voltage Law (KVL) and the principle of voltage division in DC series circuits
2. To verify Kirchhoff's Current Law (KCL) and the principle of current division in DC parallel circuits.
3. To understand the concept of node analysis of DC circuits
4. To understand the concept of Thevenin's theorem
5. To understand the concept of Norton's theorem, and
6. To understand the concept of Superposition theorem

**Laboratory Exercise Procedure**:

**1.** Choose six resistors as assigned. Most should be in the range from 1 kΩ to 10 kΩ. Determine the resistor's "nominal" value for each resistor using the color code. Measure the resistance value of each resistor using the laboratory Digital Multimeter (DMM). Enter the color code, the nominal value, and the measured value in a table. (Use these resistors for the rest of the laboratory exercise.)

**2. Kirchhoff's Voltage Law and the Voltage Division Principle**

**Theory:** Kirchhoff's Voltage Law (KVL) states that the algebraic sum of the voltages across elements around any closed path (loop) in a DC circuit is zero. Figure 2.1 shows a DC circuit in which a few resistors are connected in series across a source whose Voltage is $V_S$. Using the convention that the Voltage drop across each component in the clockwise path around the loop is positive, the KVL equation is given below. Note the negative sign for Vs, a positive Voltage, and hence a negative "drop."

$$-V_s + V_1 + V_2 + V_3 \ldots\ldots + V_N = 0 \text{ V} \qquad (2.1)$$

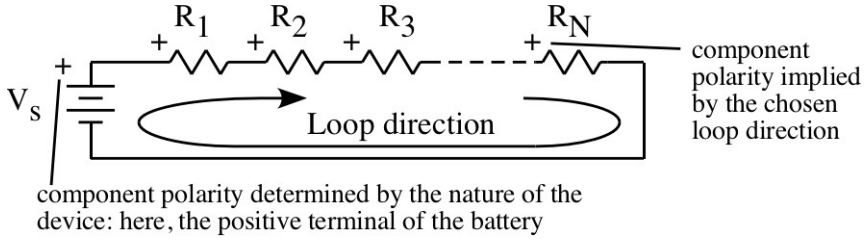


Figure 2.1 DC series circuit

According to the Voltage division principle, the Voltage drop across any resistor in a DC series circuit is proportional to the value of that resistor. Referring to Figure 2.1, the Voltage drop $V_X$ across any resistor $R_X$ can be shown to be:

$$V_X = (V_S / R_{eq}) R_X \qquad (2.2)$$

where the equivalent (total) resistance of the circuit is given by:

$$R_{eq} = R_1 + R_2 + ... + R_N \qquad (2.3)$$

**Procedure:** Choose three resistors from your collection (as assigned) and connect them in series to a DC Voltage source as shown in Figure 2.1. Supply a suitable Voltage (about 8 to 15 Volts) using the DC power supply. Measure the source Voltage $V_S$ and the Voltage across each resistor using the DMM for all measurements. Enter the readings in a table.

Make the following Calculations, adding appropriate calculated values to your table:

1. To verify KVL, calculate the sum of the Voltage drops across the resistors in the circuit and check to see whether this is equal to the source Voltage.
2. To verify the Voltage division principle, calculate the Voltage drop across each resistor using equation (2.2) and verify (1) whether the calculated and measured values agree, and (2) whether the Voltage drops are proportional to resistor values.

3. **Kirchhoff's Current Law** and the **Current Division Principle**

**Theory**: Kirchhoff's Current Law (KCL) states that the algebraic sum of the currents at any node in an electric circuit is zero.

Referring to Figure 2.2, using the convention that the current entering a node is (say) negative and that leaving the node is positive, the KCL equation is: (Note also that $I_S = I_1$.)

$$-I_S + I_2 + I_3 = 0A \qquad (2.4)$$

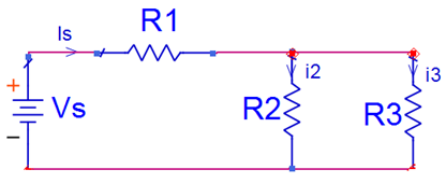


Figure 2.2 Currents at a node of a DC circuit

According to current division principle, the current through a resistor in a DC parallel circuit is inversely proportional to its resistance value.

Referring to Figure 2.2, the current $I_X$ through resistor $R_X$ (either R2 or R3) can be shown to be

$$I_X = (I_S R_{eq} / R_X) \quad (2.5)$$

where Req is the equivalent resistance of just the part of the circuit including only R2 and R3 (not R1!) is related by the general case equation:

$$(1/R_{eq}) = (1/R_1) + (1/R_2) + (1/R_3) \ldots + (1/R_N) \quad (2.6)$$

In this case, there are only two resistors in parallel, so $(1/R_{eq}) = (1/R_2) + (1/R_3)$.

This can be algebraically simplified to: $R_{eq} = (R_2 R_3) / (R_2 + R_3)$

**Procedure**: Choose three resistors from your collection (as directed) and connect them (and the DMM to measure current, measuring the current through each resistor, $R_1$ to $R_3$, one at a time) to a DC voltage source as shown in Figure 2.2. Enter your measurements in a table.

Make the following calculations:

1. To verify KCL, calculate the sum of the currents through each of the parallel resistors, adding those calculated values to your table, and check to see whether the sum of the branch resistor $R_2$ and $R_3$ currents is equal to the current from the source (the same as the current through $R_1$).

2. To verify the current divider principle, calculate the current through each resistor, entering the calculated values into your table, and verify (1) whether the calculated and the measured values of currents agree, and (2) whether the currents in the resistors that are in parallel are inversely proportional to the respective resistor values.

**4. Node Analysis**

**Theory:** In a circuit with N nodes, one node can be chosen as a reference node ("ground") and an arbitrary Voltage (usually zero) assigned to it. If the voltages at the remaining (N-1) nodes are unknown, then KCL equations can be written at these (N-1) nodes, and the resulting (N-1) simultaneous equations can be solved for (N-1) unknown node Voltages. Any branch current can then be calculated using Ohm's Law. In Figure 2.3, there are three nodes other than ground. However, in this case, one of the non-ground nodes is known, since $V_S$=20V. So, we get N = 2.

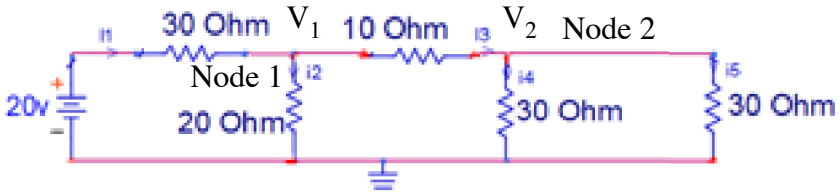


Figure 2.3 Circuit to explain node analysis

Establishing the reference (ground) node is a necessary first step. Voltages of other nodes are with respect to the reference ground (0 Volts). A "node Voltage" is measured from the node to ground. Skipping the known node at the Voltage source, KCL equations for the arbitrary (left to right, top to bottom) current directions shown are:

$$\text{Node 1: } -\frac{(20V - V_1)}{30\Omega} + \frac{(V_1 - 0V)}{20\Omega} + \frac{(V_1 - V_2)}{10\Omega} = 0V \quad (2.7)$$

$$\text{Node 2: } -\frac{(V_1 - V_2)}{10\Omega} + \frac{(V_2 - 0V)}{30\Omega} + \frac{(V_2 - 0V)}{30\Omega} = 0V \quad (2.8)$$

(Note that the convention used here is that a current is taken as positive when it is leaving a node and negative when it enters a node; a reversal of this convention will result in the same equation) Solving the equations simultaneously, $V_1 = 5.41$ V and $V_2 = 3.24$ V. Branch currents can then be calculated using Ohm's Law. In this example: $I_1 = (20V\text{-}5.41V)/30\Omega = 0.486$ A (or 486mA), $I_2 = 5.41V/20\Omega = 0.271$ A, and $I_4 = I_5 = 3.24V/30\Omega = 0.108$ A.

**Procedure**: You will be given a circuit by your instructor. Use the resistors you have collected (at the beginning of the laboratory exercise) and build the circuit. Connect the 'reference' node to the ground terminal of the DC power supply unit so that its voltage is zero. Supply suitable voltage(s) to the circuit using the DC power supply. Measure all the node voltages and the supply voltage(s) with reference to the ground. Switch off the supply. (KEEP THE CIRCUIT CONNECTED FOR THE NEXT STEP.)

Make calculations as follows.

(Hand in 1. With the form lab report, and 2-4 as a report due the following week.)

1. Calculate the branch currents for each resistor (using Ohm's Law for each resistor) and show them on the circuit, along with the node Voltages measured. Verify whether KCL is verified at each node. (If not, your measurements and/or calculations are wrong. You need to figure out what happened.)
2. Using the measured values of DC power supply voltage(s) and the resistor values, solve the circuit using node analysis, keeping the same reference node as in the procedure above. Verify whether the measured and calculated node Voltages agree. They should.
3. Use loop analysis to determine all the branch currents. Verify with the results found above.
4. Use computer simulation (PSpice or LTSpice) to verify your results.

**5. Thevenin's Theorem**

**Theory:** A circuit of linear elements and sources as in Figure 2.4 (a) may be replaced by an equivalent circuit as shown in Figure 2.4 (b) consisting of a Voltage source of Voltage $V_{Th}$, called the Thevenin Voltage, in series with a resistance $R_{Th}$, called the Thevenin resistance.

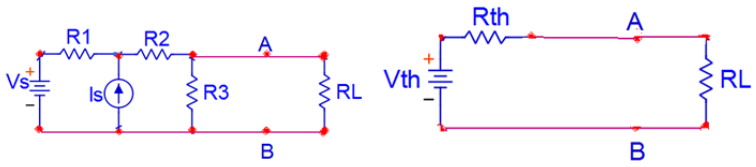


Figure 3.4 (a) Linear circuit (b) Thevenin equivalent circuit

The Thevenin Voltage is obtained by removing the 'load' resistor and measuring the open circuit voltage across the terminals A and B. The Thevenin resistance is obtained by REPLACING the voltage source(s) by short circuit(s), and any current source(s) by an open circuit, and measuring the resistance, as seen looking in from the terminals A-B (Without $R_L$).

**Procedure:** Use the SAME circuit connected for node analysis. One of the resistors will have been designated as the "load" resistor. (Be sure this resistor is identified as the "load" in the circuit schematic in your report.) Remove this resistor and connect a Voltmeter (Use the lab DMM) in its place. Supply the same voltage(s) as in node analysis and record the meter reading, which is the Thevenin Voltage. SWITCH OFF THE SUPPLY. REMOVE THE WIRE(S) FROM THE DC SUPPLY, AND SUBSTITUTE A SHORT CIRCUIT. ASK THE INSTRUCTOR OR THE TEACHING ASSISTANT TO CHECK THE CONNECTION BEFORE YOU TAKE THE READING. Connect the lab DMM at the terminals of the removed resistor and measure, and record, the resistance. This is the Thevenin resistance.

Perform the calculations (to be turned in with the report made the following week.)

1. Determine, using node analysis, the Thevenin voltage and verify with the measured value.
2. Determine by calculation the Thevenin resistance, and verify with the measured value.
3. Calculate the current through the 'load' resistor as $V_{Th}/(R_{Th}+R_L)$ and compare with the current determined by node analysis in the previous Node Analysis section

6. **Norton's Theorem**

**Theory:** A circuit of linear elements and sources, as in Figure 3.4 (a), may be replaced by an equivalent circuit as shown in Figure 2.5 consisting of a current source of current $I_N$, called the Norton's current, in parallel with Thevenin (or called Norton, having the same value) resistance

$R_{Th}$. Norton's current is obtained by replacing the 'load' resistor by an ammeter and measuring the 'short circuit' current flowing from terminal A to terminal B.

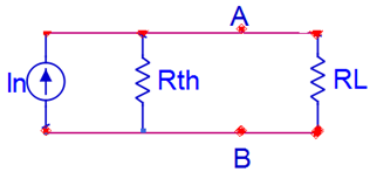


Figure 2.5 Norton's equivalent circuit

**Procedure:** Use the SAME circuit connected for node analysis. Remove the 'load' resistor and connect an ammeter (DMM configured for current) in its place. Supply the same voltage(s) as in the node analysis. Measure and record the meter reading, which is the Norton's current.

Perform the calculations below (to be turned in as part of report the following week):

1. Determine the Norton's current by analysis with RL shorted. Verify against measured value.
2. Verify whether $I_N = V_{Th}/R_{Th}$.

**7. Superposition Theorem**

**Theory:** The current or voltage associated with any branch in a linear network equals the sum of the current or voltage components set up in that branch due to each of the *independent* sources acting one at a time in the circuit. A linear network is a circuit in which all of the components are "linear" the same way a resistor is. (You will later see that capacitors and inductors are also linear components. Diodes are not linear. So superposition might not hold for a circuit that includes diodes.) Example of figure 2.6 below shows a case with two sources:

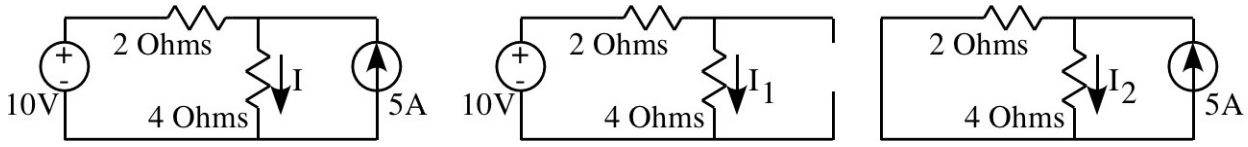


Figure 2.6. Circuit to explain superposition theorem

Current I = $I_1$ (due to 10 V source alone with the current source opened or zero) + (plus)

$I_2$ (due to 5 A source alone with the voltage source shorted or zero)

**Procedure**: Use the SAME circuit connected for node analysis. Keep one of the two voltage sources, remove the other source, and short circuit the terminals (at the circuit) as you did in the procedure to find Thevenin resistance. Adjust the supply voltage to the same value used in node

analysis for verification of results. Note down the current in ANY resistor and Voltage at any node. Switch off the supply. Repeat the procedure by connecting the second source and removing the first source and short circuiting the terminals. Note down the current through the **same** resistor and the Voltage at the **same** node as in the previous step. Switch off the supply. (If the circuit used for node analysis had only one power supply connection, instead set that supply to two different Voltages which total the original supply Voltage used for node analysis. That does not illustrate the principle as well as using two separate supplies.)

Perform the following calculations:

1. Verify whether the sum of the currents in the two steps match the current noted in the node analysis method; repeat this for the node voltage also. (This is turned in with the form report)
2. Determine the current (you measured) and the voltage (you measured) using circuit analysis methods for the circuit with the first voltage source alone was used. (Use the same supply Voltage you kept in the experiment for the analysis). Verify with the readings noted down.
3. Repeat the above analysis with the second source alone in the circuit. Verify with the values noted down.

**8. Reports:**

Turn in the form report for this Laboratory Exercise. This form will have the results and measurements you obtained in the laboratory. That includes all of the results from parts 1 (R measurements), 2 (KVL), 3 (KCL), lab measurements from part 4 and consistency check (Node Analysis), measurements from Parts 5, 6, and 7 (Thevenin, Norton, Superposition)

At the beginning of Lab #3, hand in the written report for this lab exercise, which includes the circuit analysis and simulation materials associated with parts 4 to 7. The written report must include a cover page giving a title, the students' names, section, and lab station. The node analysis needs to include the figure showing the circuit, a table of the lab results, the calculated results from node and loop analysis, and simulation results. These need to be presented in a manner to make a comparison easy. Append the simulation schematic and results image for the node analysis circuit. It should look something like Figure 2.7 below (from ORCAD/PSpice):

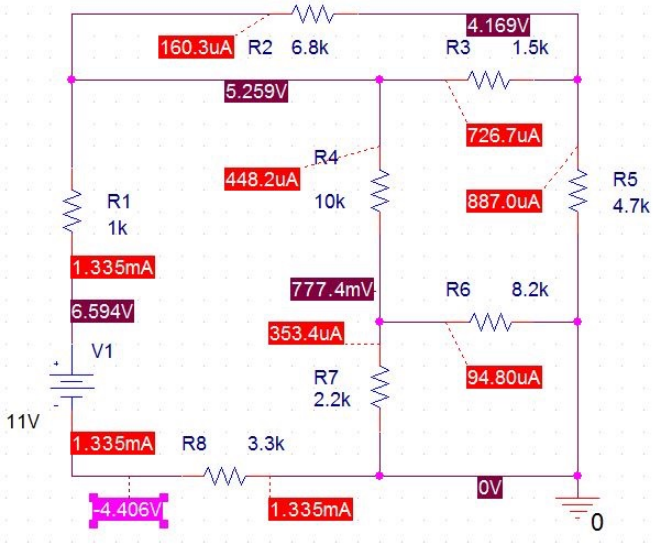


Figure 2.7 Example of DC Circuit Simulation Circuit and Results